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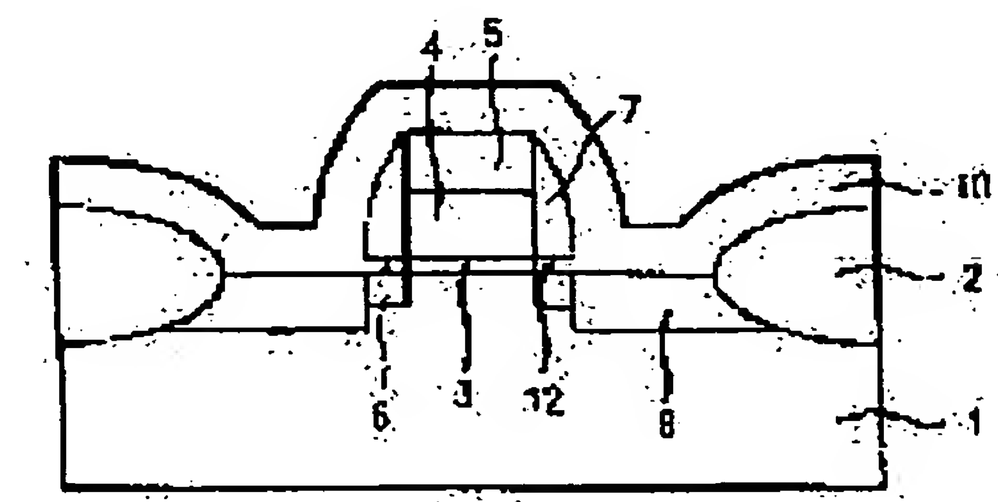
(54) FABRICATION OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To enhance the characteristics of a device by forming a gate insulation film only at the width of a gate electrode and forming an air gap between semiconductor substrate on the opposite sides thereof and the sidewall of the insulation film, thereby eliminating electron trouble of the gate insulation film on the side face of gate.

SOLUTION: An MOSFET has structures consisting of a gate insulation film 3, a gate electrode 4 and a cap gate insulation film 5 are formed at a specified part in an active region defined by a field oxide 2 deposited on a p-type semiconductor substrate 1. An insulation film sidewall 7 is formed on the side face of the gate electrode 4, and the cap gate insulation film 5 and an air gap 12 is formed at least partially between the insulation film sidewall 7 and the semiconductor substrate 1 on the opposite sides of the gate insulation film 3. The gate insulation film 3 is formed of an oxide, and time insulation film side wall 7 is formed of a nitride having an etching selection rate different from that of the gate insulation film 3.



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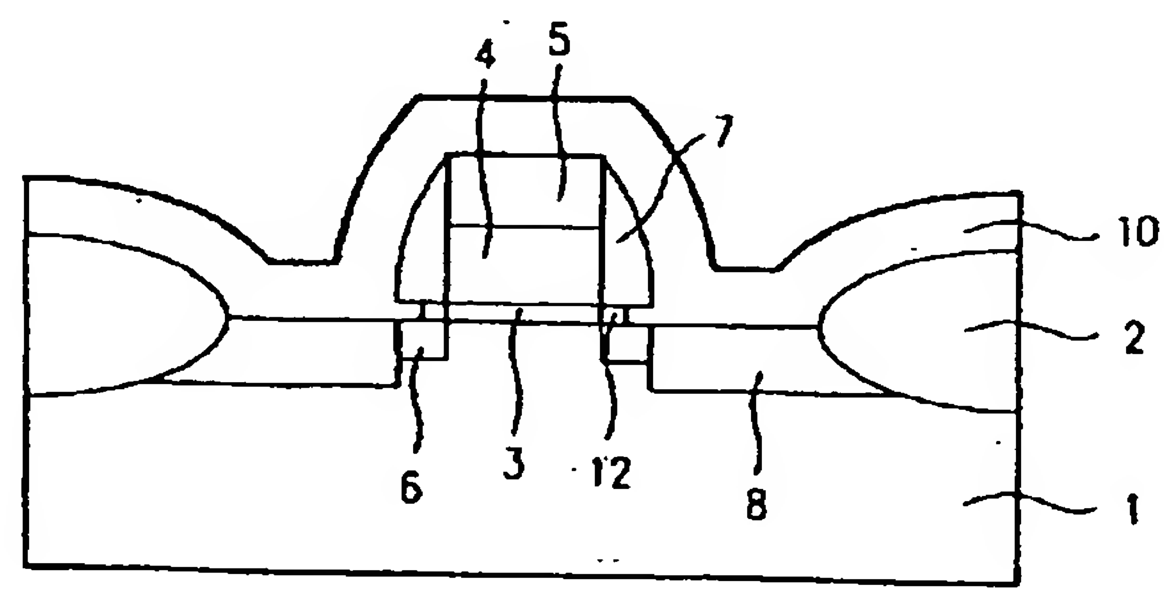
(54)【発明の名称】　半導体デバイス及び製造方法

(57)【要約】

【課題】　ゲート絶縁膜側壁での電子トラップを防止したＭＯＳ電界効果トランジスタ及びその製造方法を提供する。

【解決手段】　本発明は、第１導電型半導体基板上に順次に形成されるゲート絶縁膜及びゲート電極と、ゲート電極の側面に形成される絶縁膜側壁とを備えた半導体デバイスであって、ゲート絶縁膜をゲート電極の幅にのみ形成させ、その両側の半導体基板と絶縁膜側壁との間に空隙を形成させたことを特徴とする半導体デバイス。



【特許請求の範囲】
【請求項１】 第１導電型半導体基板上に順次に形成されるゲート絶縁膜及びゲート電極と、ゲート電極の側面に形成される絶縁膜側壁とを備えた半導体デバイスであって、ゲート絶縁膜をゲート電極の幅にのみ形成させ、その両側の半導体基板と絶縁膜側壁との間に空隙を形成させたことを特徴とする半導体デバイス。
【請求項２】 前記ゲート電極と第１絶縁膜側壁との間に第２絶縁膜側壁が更に形成されていることを特徴とする請求項１記載の半導体デバイス。
【請求項３】 第１導電型半導体基板上にゲート絶縁膜を形成する段階と、
ゲート絶縁膜上にゲート電極を所定の大きさに形成する段階と、
ゲート電極の側面に絶縁膜側壁を形成する段階と、
絶縁膜側壁の形成のときに露出したゲート絶縁膜と絶縁膜側壁の下側のゲート絶縁膜を選択的に除去する段階と、
絶縁膜側壁の下側のゲート絶縁膜が除去された部分が完全に埋め込まれないようにゲート電極を含む半導体基板の全面に絶縁膜を形成する段階とを備えることを特徴とする半導体デバイスの製造方法。
【請求項４】 前記ゲート絶縁膜と絶縁膜側壁とは互いに異なるエッチング選択比を有する絶縁物質により形成されることを特徴とする請求項３記載の半導体デバイスの製造方法。
【請求項５】 第１導電型半導体基板上の所定部位に順次にゲート絶縁膜、ゲート電極、及びキャップゲート絶縁膜を形成する段階と、
ゲート絶縁膜のゲート電極の下側以外の部分を除去してゲート電極の両側表面及び半導体基板の表面に第１絶縁膜を形成する段階と、
前記半導体基板のゲート電極の両側に低濃度第１導電型不純物領域を形成する段階と、
前記キャップゲート絶縁膜及び第１絶縁膜の側面に絶縁膜側壁を形成する段階と、
前記絶縁膜側壁の形成によって露出された第１絶縁膜を除去し、かつ絶縁膜側壁の下側の第１絶縁膜を選択的に除去する段階と、
前記第１絶縁膜を選択的に除去した後、キャップゲート絶縁膜及び絶縁膜側壁を含む半導体基板の全面に第２絶縁膜を絶縁膜側壁の下側の第１絶縁膜の除去された部分に空隙ができるように形成する段階と、を備えることを特徴とする半導体デバイスの製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体デバイス及びその製造方法に関し、特にゲート絶縁膜の側壁での電子トラップ及びゲート絶縁膜とシリコン基板の間の界面で生じる悪影響を防止することができるＭＯＳ電界効果トランジスタ（ＭＯＳＦＥＴ）及びその製造方法に関する。
【０００２】
【従来の技術】一般に、ＭＯＳデバイスは、半導体Ｓｉの表面に酸化膜SiO_2を形成し、その上に金属を形成した構造である。そのうち電界効果トランジスタは、第１導電型シリコン基板に酸化膜からなるゲート絶縁膜及びゲート電極が順次に形成され、シリコン基板のゲート電極の両側にソース／ドレイン不純物領域が形成されている。このＭＯＳＦＥＴはゲート電極の電位に基づいてソース－ドレイン間に流れる電流（チャネル電流）を制御することができる。
【０００３】以下、従来のＭＯＳＦＥＴを図面に基づき説明する。図１は従来のＭＯＳＦＥＴの構造平面図であり、図２は図１のＩ－Ｉ’線上の構造断面図であり、図３は図１のII－II’線上の構造断面図であり、図４ａ～図４ｄは図１のＩ－Ｉ’線上の従来のＭＯＳＦＥＴの工程断面図である。従来のｎチャネルＭＯＳＦＥＴの構造は、ｐ型半導体基板１のフィールド領域にフィールド酸化膜２が形成され、アクティブ領域の所定部位にゲート絶縁膜３、ゲート電極４、及びキャップゲート絶縁膜５が形成される。そして、ゲート絶縁膜３、ゲート電極４、及びキャップゲート絶縁膜５の側面には絶縁膜側壁７が形成され、半導体基板１の絶縁膜側壁７の下には低濃度ｎ型不純物領域６が、かつ絶縁膜側壁７の両側にはソース／ドレイン領域である高濃度ｎ型不純物領域８が形成される。
【０００４】かかる構造を有する従来のｎチャネルＭＯＳＦＥＴの製造方法を図４ａ～図４ｄに基づき説明する。図４ａに示すように、ｐ型半導体基板１のフィールド酸化膜２で区画したアクティブ領域に酸化膜でゲート絶縁膜３を形成する。図４ｂに示すように、ゲート絶縁膜３の所定部位にゲート電極４及びキャップゲート絶縁膜５を順次に形成し、これらのゲート電極４及びキャップゲート絶縁膜５をマスクに用いて低濃度ｎ型不純物イオンを注入する。
【０００５】図４ｃに示すように、全面に絶縁膜を堆積し異方性エッチングしてゲート電極４及びキャップゲート絶縁膜５の側面に絶縁膜側壁７を形成する。そして、図４ｄに示すように、キャップゲート絶縁膜５及び絶縁膜側壁７をマスクに用いた高濃度ｎ型不純物イオン注入で半導体基板１の絶縁膜側壁７の両側にソース／ドレイン領域である高濃度ｎ型不純物領域８を形成する。
【０００６】従来のＭＯＳＦＥＴは、ゲート電極４及び絶縁膜側壁７と半導体基板１との間に酸化膜からなるゲート絶縁膜３が形成され、ソース／ドレイン領域が低濃度不純物領域６と高濃度不純物領域８とからなるＬＤＤ ＭＯＳＦＥＴである。これにより、ゲート電極４にしきい値電圧以上の電圧を印加すると、ゲート電極４の下側の半導体基板にチャネルが形成されてソース及びドレ

イン領域間に電流が流れる。このとき、従来のＬＤＤ構造のＭＯＳＦＥＴは、既存のドレイン・ソースが単一に形成されたＭＯＳＦＥＴより、低濃度不純物領域の抵抗によりゲート電極のエッジでのドレイン電界を減少させ得る。従って、デバイス動作時のホットキャリヤによる特性の低下を改善することができるという利点を備えている。

【０００７】

【発明が解決しようとする課題】しかし、上述した従来のＭＯＳＦＥＴは、絶縁膜側壁と半導体基板との間に酸化膜が形成されているので、ＭＯＳＦＥＴの動作時に絶縁膜側壁の下側の酸化膜とシリコン基板との間の界面及び酸化膜内に電荷トラップが発生するため、デバイスの特性が低下する問題点があった。本発明は上記の問題点を解決するためになされたものであり、その目的はゲート側面のゲート絶縁膜で発生する電子トラップを防止してデバイスの特性を向上させることができるＭＯＳＦＥＴ及びその製造方法を提供することにある。

【０００８】

【課題を解決するための手段】上記目的を達成するための本発明の半導体デバイスは、第１導電型半導体基板上に順次に形成されるゲート絶縁膜及びゲート電極と、ゲート電極の側面に形成される絶縁膜側壁とを備えたデバイスであって、ゲート絶縁膜をゲート電極の幅にのみ形成させ、その両側の半導体基板と絶縁膜側壁との間に空隙を形成させたことを特徴とするものである。

【０００９】上記目的を達成するための本発明の半導体デバイスの製造方法は、第１導電型半導体基板上にゲート絶縁膜を形成する段階と、ゲート絶縁膜上にゲート電極を所定の大きさに形成する段階と、ゲート電極の側面に絶縁膜側壁を形成する段階と、絶縁膜側壁の形成のときに露出したゲート絶縁膜と絶縁膜側壁の下側のゲート絶縁膜を選択的に除去する段階と、絶縁膜側壁の下側のゲート絶縁膜が除去された部分が完全に埋め込まれないようにゲート電極を含む半導体基板の全面に絶縁膜を形成する段階とを備えることを特徴とする。

【００１０】

【発明の実施形態】以下、本発明の半導体デバイス及びその製造方法を添付図面に基づき詳細に説明する。図５は本発明の第１実施形態のＭＯＳＦＥＴの構造平面図であり、図６は図５のＩ－Ｉ’線上のＭＯＳＦＥＴの構造断面図であり、図７は図５のII－II’線上のＭＯＳＦＥＴの構造断面図であり、図８ａ～図８ｄは図５のＩ－Ｉ’線上の本発明の第１実施形態のＭＯＳＦＥＴの工程断面図である。本第１実施形態のＭＯＳＦＥＴの構造は、ｐ型半導体基板１に形成させたフィールド酸化膜２で区画したアクティブ領域の所定部位にゲート絶縁膜３、ゲート電極４、及びキャップゲート絶縁膜５が形成される。本実施形態においては、ゲート絶縁膜はアクティブ領域前面に形成させずに、ゲート電極４の下側にのみ形成させる。そして、ゲート電極４及びキャップゲート絶縁膜５の側面には絶縁膜側壁７が形成されるが、この絶縁膜側壁７と半導体基板１との間の少なくとも一部、ゲート絶縁膜３の両側に空隙１２を形成させている。ゲート絶縁膜３は酸化膜で形成され、絶縁膜側壁７はゲート絶縁膜３とエッチング選択比が異なる窒化膜で形成される。従来同様、絶縁膜側壁７の下側の半導体基板１には低濃度ｎ型不純物領域６が形成され、絶縁膜側壁７の両側の半導体基板１にはソース／ドレイン領域である高濃度ｎ型不純物領域８が形成される。キャップゲート絶縁膜５、絶縁膜側壁７、高濃度ｎ型不純物領域８、及びフィールド酸化膜２の表面に絶縁膜１０が形成される。この絶縁膜１０の形成にあたっては、絶縁膜１０がゲート電極４の下側にのみ形成させたゲート絶縁膜３にまで達しないようにし、絶縁膜側壁の下側に半導体基板１との間に空隙１２を形成する。

【００１１】次ぎに上記構造を有する本第１実施形態のＭＯＳＦＥＴの製造方法を図８に基づいて説明する。図８ａに示すように、ｐ型半導体基板１のフィールド領域にフィールド酸化膜２を形成し、アクティブ領域に酸化膜でゲート絶縁膜３を形成し、ゲート絶縁膜３の上に所定の幅でゲート電極４とキャップゲート絶縁膜５を順次に形成する。ゲート絶縁膜とキャップゲート絶縁膜５は酸化膜で形成する。ゲート電極４及びキャップゲート絶縁膜５をマスクに用いて半導体基板１に低濃度ｎ型不純物イオンを注入して低濃度ｎ型不純物領域６を形成する。

【００１２】図８ｂに示すように、ゲート絶縁膜３とはエッチング選択比の異なる、例えば窒化膜等の絶縁膜を全面に堆積し、異方性エッチングでゲート電極４及びキャップゲート絶縁膜５の側面に絶縁膜側壁７を形成する。その後、絶縁膜側壁７をマスクに用いて露出されたゲート絶縁膜３をも除去する。絶縁膜側壁７及びキャップゲート絶縁膜５をマスクに用いた高濃度ｎ型不純物イオン注入で前記絶縁膜側壁７の両側の前記半導体基板１にソース／ドレイン領域の高濃度ｎ型不純物領域８を形成する。

【００１３】図８ｃに示すように、全面に感光膜９を堆積し、アクティブ領域上のキャップゲート絶縁膜５、ゲート電極４、絶縁膜側壁７、及び絶縁膜側壁７に隣接する高濃度ｎ型不純物領域８の所定部分が露出されるようにパターニングし、絶縁膜側壁７の下側のゲート絶縁膜３を選択的に除去する。ゲート絶縁膜３は湿式エッチングにより除去される。上記のように、この実施形態ではゲート絶縁膜を２度にわたって除去しているが、１度のエッチングで側壁７の下側のものが除去されるまで行っても良い。なお、キャップゲート絶縁膜５はゲート絶縁膜の除去によっても除去されない程度に予め堆積しておく。また、キャップゲート絶縁膜と側壁とを同じ窒化膜で形成させてもよい。図８ｄに示すように、感光膜９を

全部除去し、キャップゲート絶縁膜５、絶縁膜側壁７を含む基板の全表面に絶縁膜１０を形成する。このとき、絶縁膜１０は絶縁膜側壁７と半導体基板１との間に完全には入り込まず、ゲート絶縁膜３と絶縁膜１０の間であって、絶縁膜側壁７と基板１との間に空隙１２が形成される。すなわち、ゲート電極の両側に空隙１２が形成される。

【００１４】さらに、本発明の第２実施形態の半導体デバイス及びその製造方法は次の通りである。図９は本第２実施形態のＭＯＳＦＥＴの構造平面図であり、図１０は図９のＩ－Ｉ’線上のＭＯＳＦＥＴの構造断面図であり、図１１は図９のII－II’線上のＭＯＳＦＥＴの構造断面図であり、図１２ａ～図１２ｄは図９のＩ－Ｉ’線上の本発明の第２実施形態のＭＯＳＦＥＴの工程断面図である。本発明の第２実施形態のＭＯＳＦＥＴの構造は、先に説明した第１実施形態の構造においてゲート電極と絶縁膜側壁との間に他の絶縁膜側壁を形成したのである。すなわち、第２実施形態のＭＯＳＦＥＴの構造は、絶縁膜側壁を第１実施形態と同じ絶縁材からなる第１絶縁膜側壁７とその側壁とゲート電極４の両側面との間に他の材質からなる第２絶縁膜側壁１１ａを形成させたことが第１実施形態と異なるだけで他は同じである。

【００１５】かかる構造を有する本発明の第２実施形態のＭＯＳＦＥＴの製造方法は以下の通りである。図１２ａに示すように、ｐ型半導体基板１のフィールド領域にフィールド酸化膜２を形成する。アクティブ領域の半導体基板１の所定部位にゲート絶縁膜３、ゲート電極４、及びキャップゲート絶縁膜５を順次に形成する。その後ゲート絶縁膜３をゲート電極４の下側の部分を除去して基板表面を露出させる。ゲート電極４の側面及び露出された半導体基板１の表面に薄い酸化膜等の第１絶縁膜１１を形成する。この第１絶縁膜１１は熱酸化方法により酸化膜で形成する。ゲート電極４及びキャップゲート絶縁膜５をマスクに用いて半導体基板１のゲート電極４の両側に低濃度ｎ型不純物イオンを注入して低濃度ｎ型不純物領域６を形成する。

【００１６】図１２ｂに示すように、全面に絶縁膜を堆積し異方性エッチングして第１絶縁膜１１及びキャップゲート絶縁膜５の側面に第１絶縁膜側壁７を形成する。この第１絶縁膜側壁７はキャップゲート絶縁膜５及び第１絶縁膜１１をエッチストッパとして利用するために窒化膜で形成する。そして、絶縁膜側壁７をマスクに用いて露出された第１絶縁膜１１を選択的に除去して基板表面を露出させる。第１絶縁膜側壁７及びキャップゲート絶縁膜５をマスクに用いた高濃度ｎ型不純物イオン注入で前記絶縁膜側壁７の両側の前記半導体基板１にソース／ドレイン領域の高濃度ｎ型不純物領域８を形成する。

【００１７】図１２ｃに示すように、全面に感光膜９を堆積し、アクティブ領域上のキャップゲート絶縁膜５、ゲート電極４、第１絶縁膜側壁７、及び第１絶縁膜側壁７に隣接する高濃度ｎ型不純物領域８の所定部分が露出されるように感光膜９をパターニングし、第１絶縁膜側壁７の下側の第１絶縁膜１１を選択的に除去して第１絶縁膜側壁７とゲート電極４との間に第２絶縁膜側壁１１ａを形成する。

【００１８】図１２ｄに示すように、感光膜９を全部除去し、キャップゲート絶縁膜５、第１絶縁膜側壁７を含む基板の全表面に第２絶縁膜１０を形成する。このとき、第１絶縁膜１１が除去された部分の第１絶縁膜側壁７と半導体基板１との間は空隙１２が形成される。このように、第１絶縁膜１１を形成させてからその側壁７の下側を除去するようにすると、ゲート絶縁膜３を直接エッチングして空隙を形成させる場合に比べて、そのエッチングによる除去を制御することが容易となり、歩留まりが向上する。

【００１９】

【発明の効果】上述したように、本発明においては、絶縁膜側壁と半導体基板との間のゲート電極よりの部分の絶縁膜を除去して、そこに空隙を形成させたため、ドレイン電界によりホットキャリヤが発生しても絶縁膜側壁と半導体基板との間のトラップ発生が防止される。このため、デバイスの特性が向上する。すなわち、ゲート電極と半導体基板との間の漏洩電流を減少させることができるとともに、高いゲート電圧を使用することができる。

【００２０】また、空隙を形成させる際に、半導体基板の表面に絶縁膜を形成し、絶縁膜側壁の下側のその絶縁膜を除去するようにすると、簡単に除去することができ歩留まりが向上する。さらに、ゲート絶縁膜と絶縁膜側壁とを互いにエッチング選択比の異なる物質で形成すると、ゲート絶縁膜を選択的にエッチングすることができる。したがって、工程が容易になる。

【図面の簡単な説明】

【図１】 従来のＭＯＳＦＥＴの構造平面図。

【図２】 図１のＩ－Ｉ’線上の構造断面図。

【図３】 図１のII－II’線上の構造断面図。

【図４】 図１のＩ－Ｉ’線上の従来のＭＯＳＦＥＴの工程断面図。

【図５】 本発明の第１実施形態のＭＯＳＦＥＴの構造平面図。

【図６】 図５のＩ－Ｉ’線上のＭＯＳＦＥＴの構造断面図。

【図７】 図５のII－II’線上のＭＯＳＦＥＴの構造断面図。

【図８】 図５のＩ－Ｉ’線上の本発明の第１実施形態のＭＯＳＦＥＴの工程断面図。

【図９】 本発明の第２実施形態のＭＯＳＦＥＴの構造平面図。

【図１０】 図９のＩ－Ｉ’線上のＭＯＳＦＥＴの構造断面図。

【図１１】　図９のII－II’線上のＭＯＳＦＥＴの構造断面図。

【図１２】　図９のＩ－Ｉ’線上の本発明の第２実施形態のＭＯＳＦＥＴの工程断面図。

【符号の説明】

１　半導体基板

２　フィールド酸化膜

３　ゲート絶縁膜

４　ゲート電極

５　キャップゲート絶縁膜

６　低濃度不純物領域

７、１１ａ　絶縁膜側壁

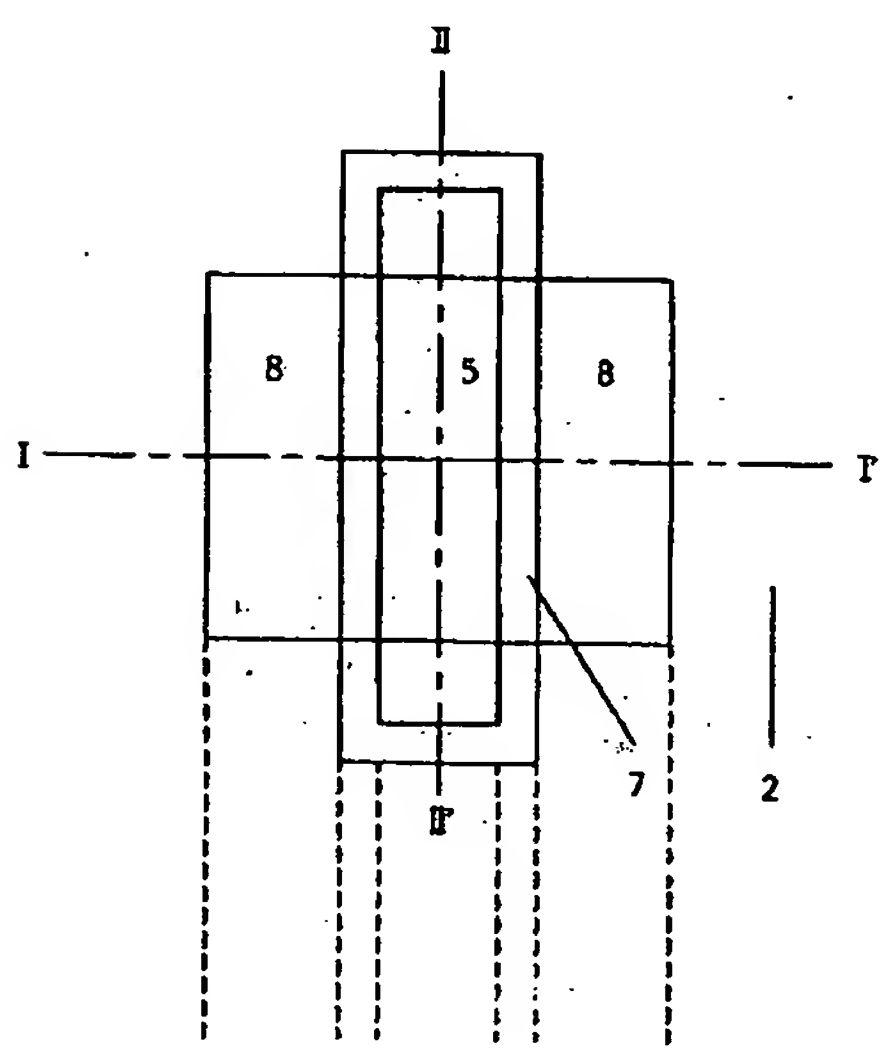
８　不純物領域

９　感光膜

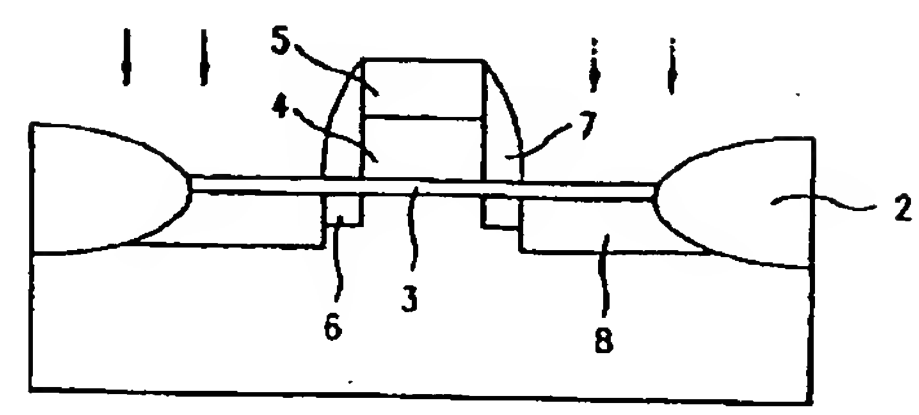
１０、１１　絶縁膜

１２　空隙

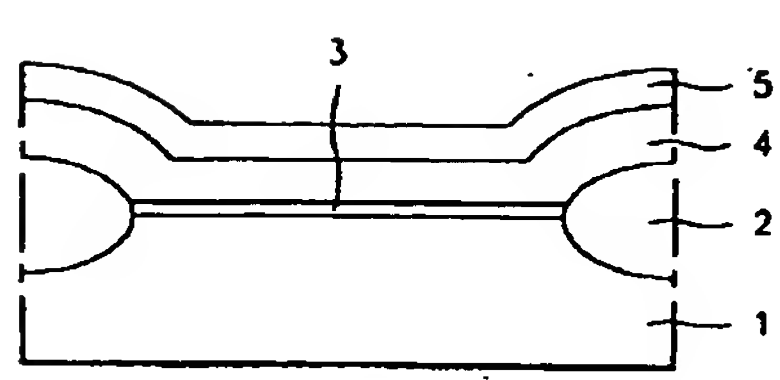
【図１】



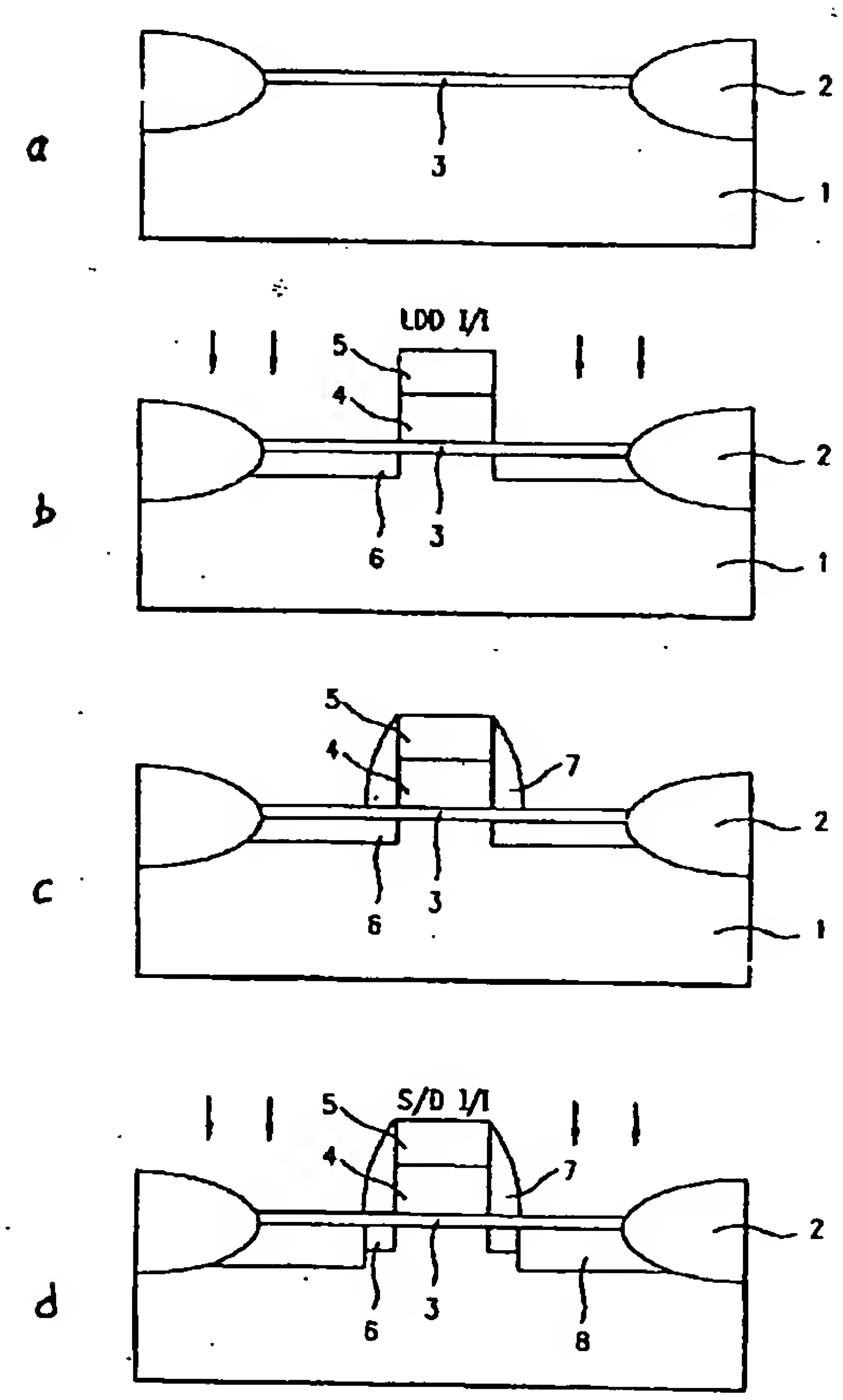
【図２】



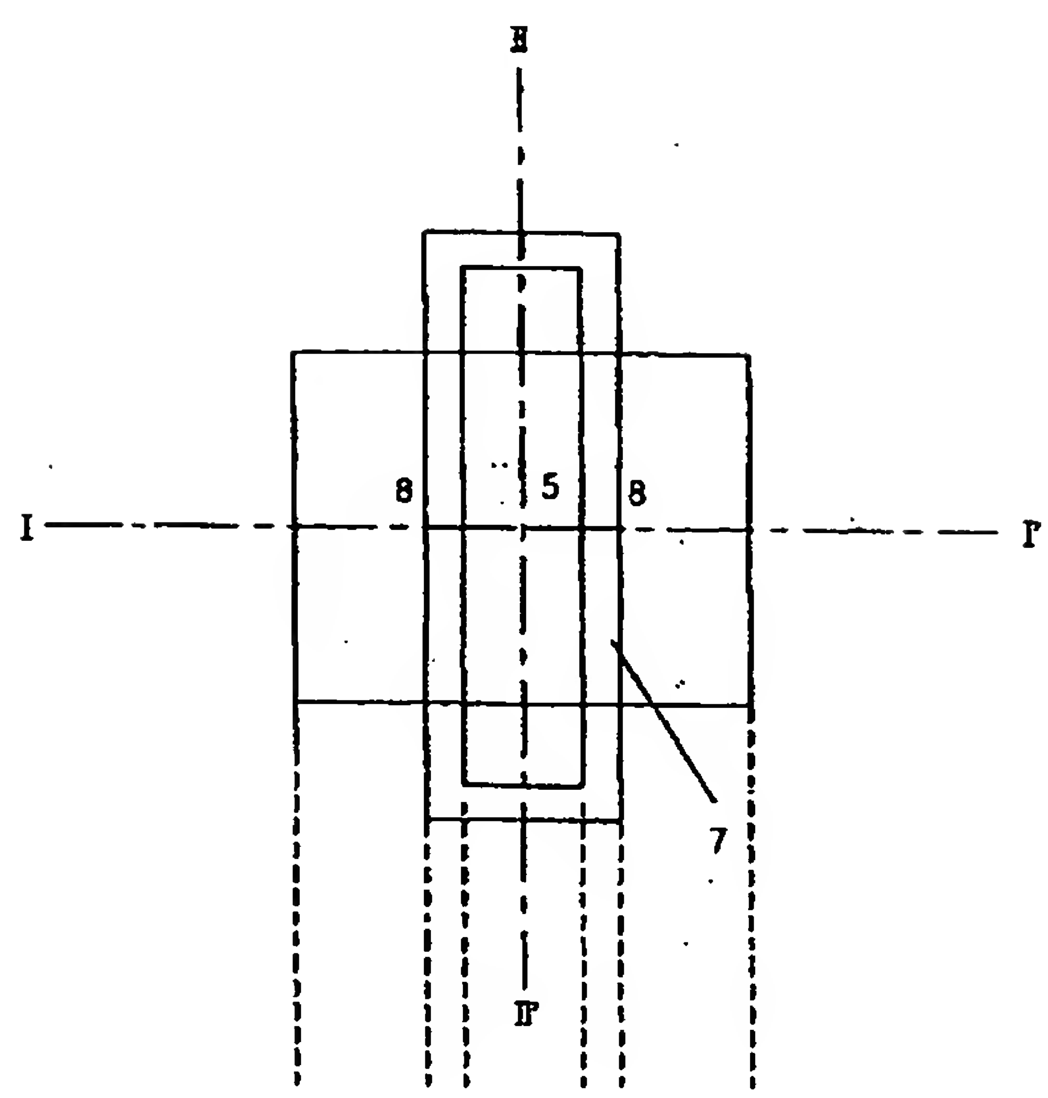
【図３】



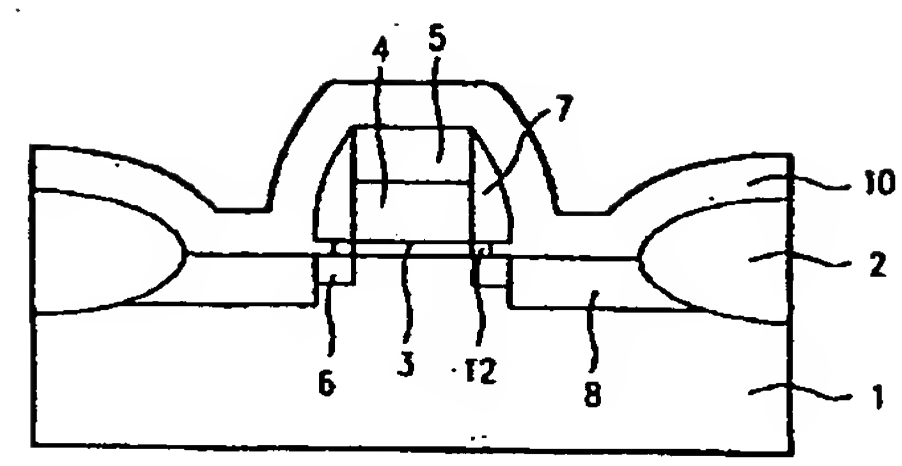
【図４】



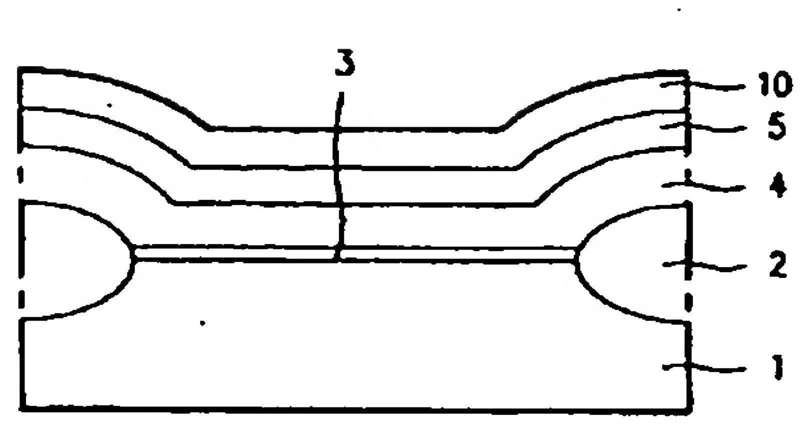
【図５】


II
I
I'
8
5
8
7
II'

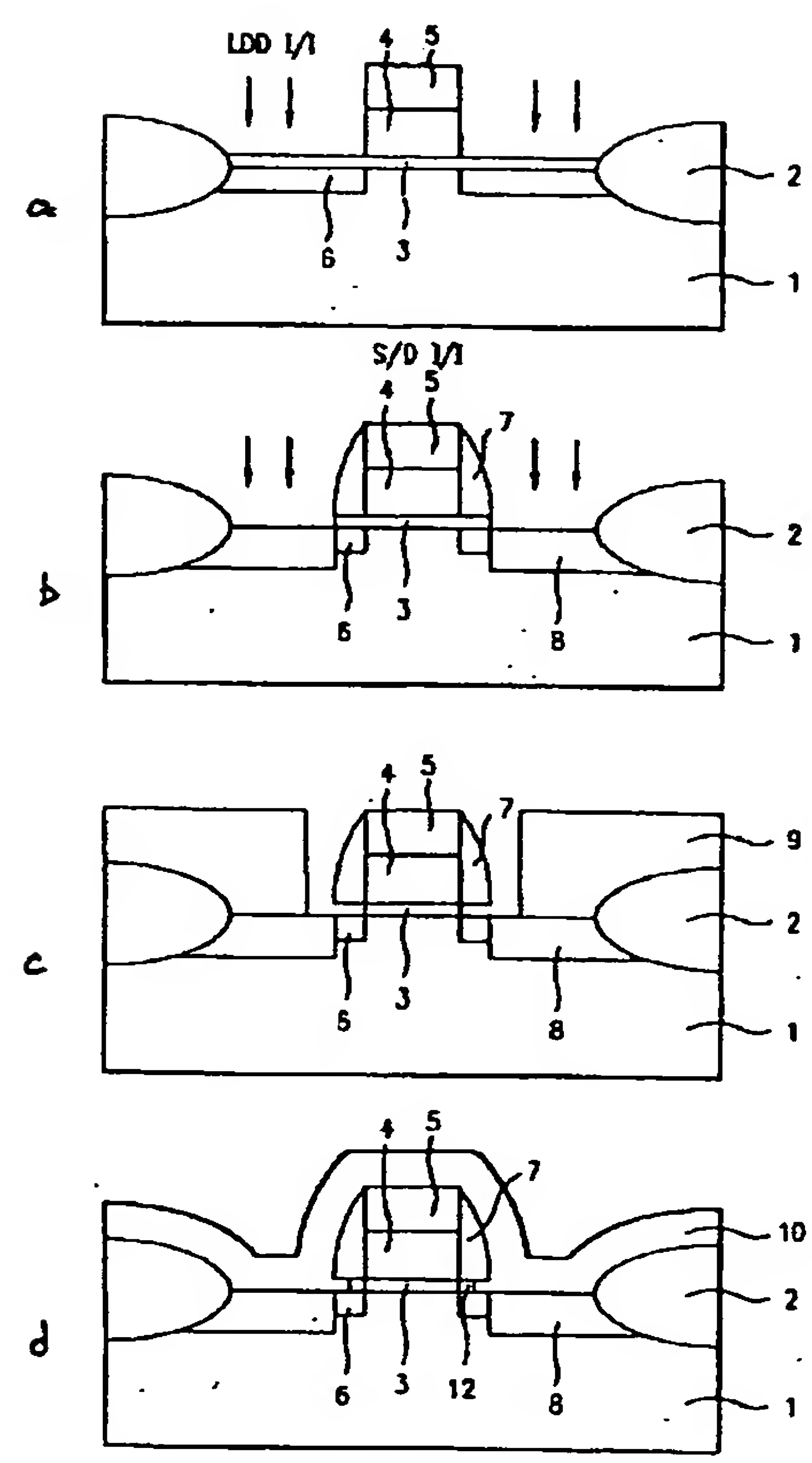
【図６】


4
5
7
10
2
6
3
12
8
1

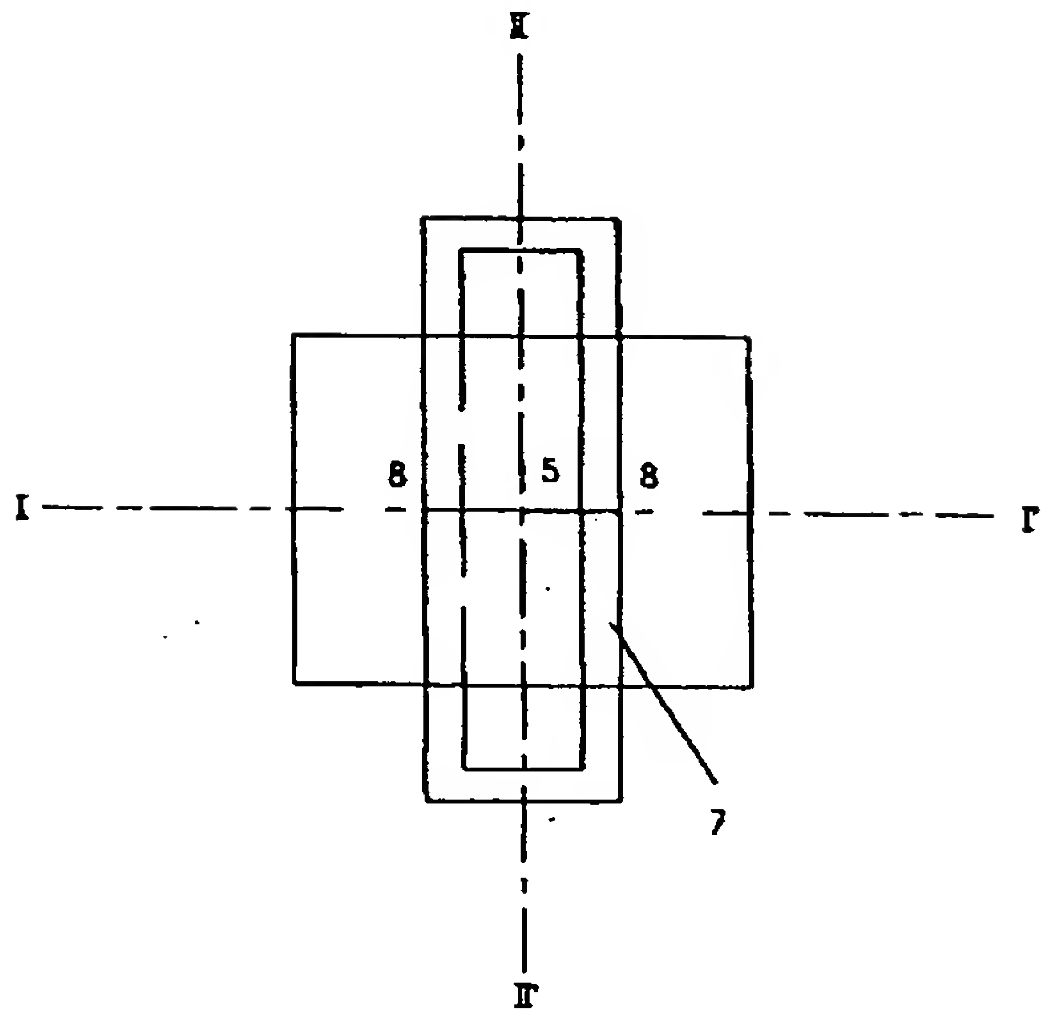
【図７】


3
10
5
4
2
1

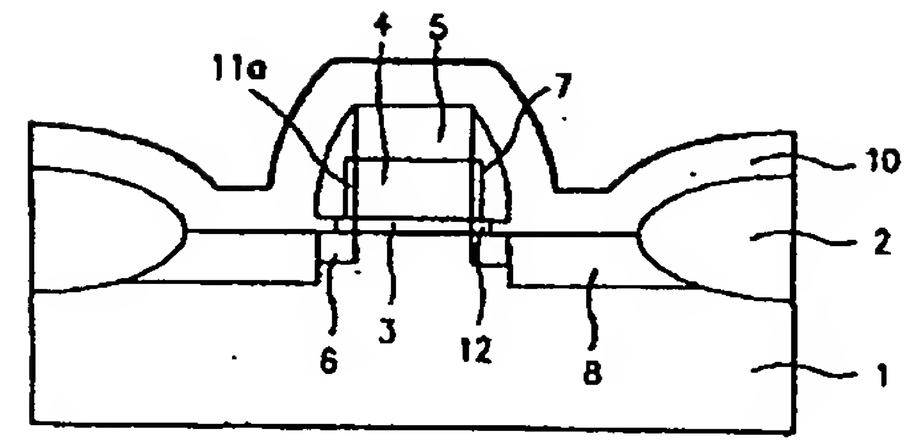
【図８】


LDD I/I
S/D I/I
a
b
c
d
4
5
7
10
9
2
6
3
12
8
1

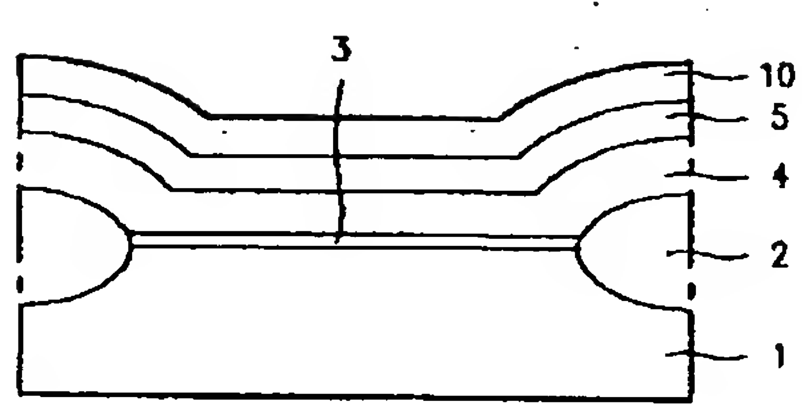
【図９】



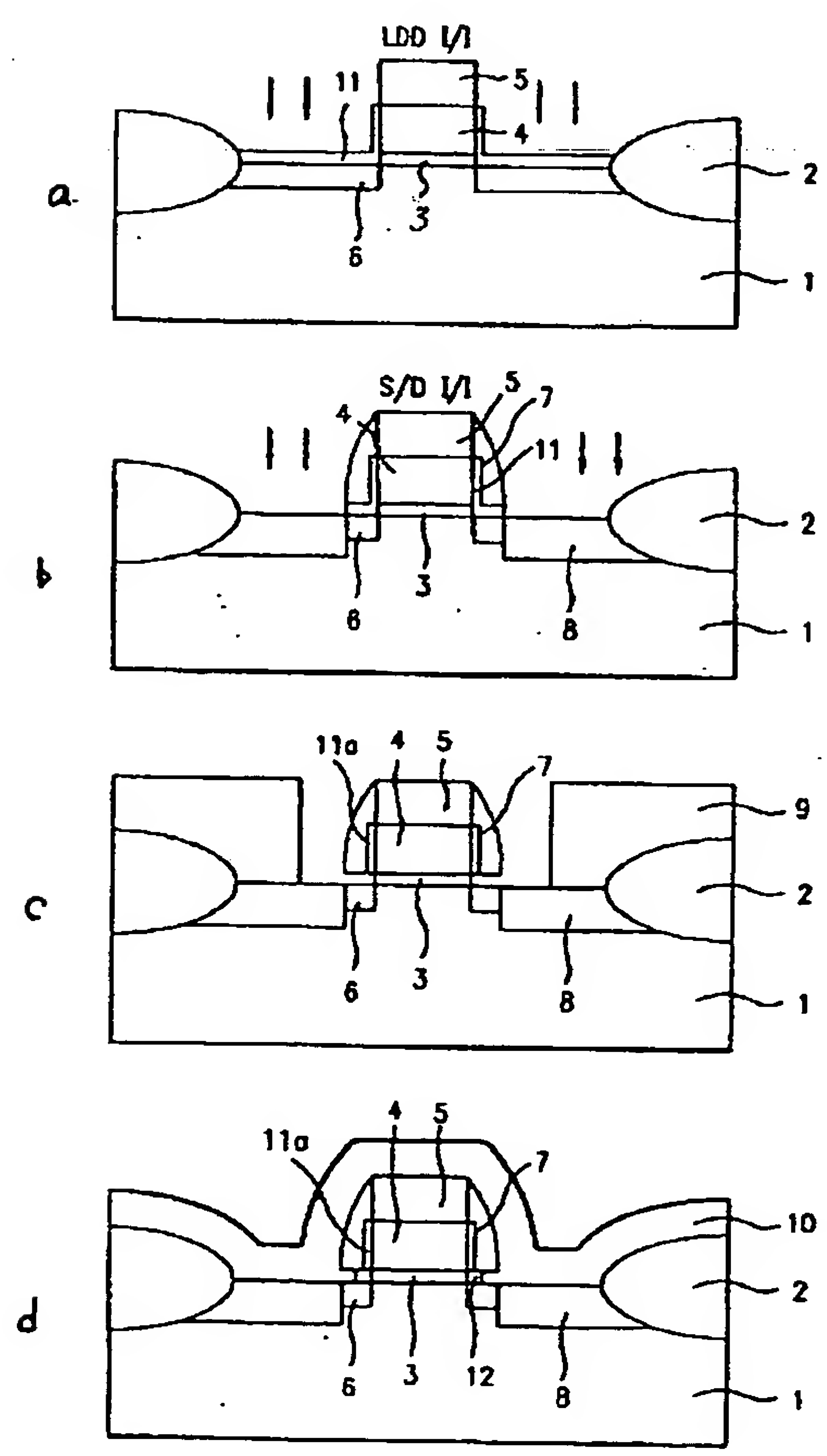
【図１０】



【図１１】



【図１２】



フロントページの続き

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１－1508

CLAIMS

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(57) [Claim(s)]
[Claim 1] The semiconductor device characterized by preventing that the hot carrier which is prepared on a semi-conductor substrate and said semi-conductor substrate, has the insulating layer which forms an opening on the field which the electric field of said semi-conductor substrate concentrate, and was generated by said opening to the field which said electric field concentrate is poured in into said insulating layer, and is captured.
[Claim 2] The semiconductor device characterized by forming the insulating thin film in equipment according to claim 1 on the field which said electric field in said opening concentrate.
[Claim 3] The semiconductor device characterized by to have the gate electrode prepared through gate dielectric film on the channel field inserted into the semi-conductor substrate, the source field and drain field established in said semi-conductor substrate front face, and said source field and a drain field, and the insulating layer which is prepared on said semi-conductor substrate and forms an opening on said channel field of said source field and a drain field, and the touching field.
[Claim 4] The semiconductor device characterized by forming the insulating thin film in equipment according to claim 3 on said source field in said opening and said channel field of a drain field, and the touching field.
[Claim 5] The semiconductor device characterized by having a semi-conductor substrate, the collector field established in said semi-conductor substrate front face, the base region which is established in said collector field front face, and consists of an external base region and an internal base region, the emitter region established in said internal base region front face, and the insulating layer which is prepared on said semi-conductor substrate and forms an opening on said internal base region.
[Claim 6] The process which forms the 1st layer alternatively on the field which the electric field of a semi-conductor substrate concentrate, The process which forms an insulating layer on said semi-conductor substrate and said 1st layer, After etching said insulating layer alternatively and exposing said a part of 1st layer, The process which forms a clearance between the field which carries out etching removal of said 1st layer alternatively using the difference of an etch rate with said insulating layer, and said electric field concentrate, and said insulating layer, The 2nd layer is deposited on the whole surface, opening of said clearance is closed, and it has the process which forms an opening on the field which said electric field concentrate. By said gap The manufacture approach of the semiconductor device characterized by preventing that the hot carrier generated to the field which said electric field concentrate is poured in into said insulating layer, and is captured.
[Claim 7] The front stirrup of the process which forms said 1st layer in an approach according to claim 6 is the manufacture approach of the semiconductor device characterized by forming said insulating thin film on the field which has the process which forms an insulating thin film on said semi-conductor substrate, and said electric field in said opening concentrate after the process which carries out etching removal of said 1st layer.
[Claim 8] The process which pours in and diffuses an impurity on said semi-conductor substrate front face by using said gate electrode as a mask, and forms a source field and a drain field after forming a

gate electrode through gate dielectric film on the channel field of a semi-conductor substrate front face, The process which forms the sidewall layer by which the laminating of the 1st and 2nd insulating layers was carried out to the touching said channel field [of said source field and a drain field], and field top, and said gate electrode side attachment wall, The difference of the etch rate of said 1st insulating layer and said 2nd insulating layer of said sidewall layer is used. The process which carries out etching removal of said 1st insulating layer alternatively, and forms a clearance between said source field and a drain field front face, and said 2nd insulating-layer base of said sidewall layer, The manufacture approach of the semiconductor device characterized by having the process which deposits the 3rd insulating layer on the whole surface, closes opening of said clearance, and forms an opening on said channel field of said source field and a drain field, and the touching field.
[Claim 9] The front stirrup of the process which forms said 1st insulating layer in an approach according to claim 8 is the manufacture approach of the semiconductor device which has the process which forms an insulating thin film on said source field and a drain field after the process which carried out etching removal of said 1st insulating layer, and is characterized by to form said insulating thin film on said source field in said opening and said channel field of a drain field, and the touching field.
[Claim 10] The process which forms the collector field which consists of a semi-conductor of the 1st conductivity type, and the process which forms the base electrode which consists of a polish recon layer by which the impurity of the 2nd conductivity type was doped on said collector field, The process which etches alternatively said predetermined insulating layer and said 1st predetermined base electrode of a location on said collector field, and forms opening after forming the 1st insulating layer in the whole surface, The process which forms the 2nd insulating layer in said collector field top in said opening, and said base-electrode side attachment wall, The process which injects the impurity ion of the 2nd conductivity type into said collector field front face of said opening circles alternatively by using said 1st insulating layer as a mask, The process which forms the 1st sidewall layer in said 1st [the] of said opening circles, and the 2nd insulating-layer side attachment wall, The difference of an etch rate with said 1st insulating layer and said 1st sidewall layer is used. The process which carries out etching removal of said 2nd insulating layer alternatively, and forms a gap between said collector field front face and said 1st sidewall layer base, The process which forms the 2nd sidewall layer in said 1st sidewall layer side attachment wall, closes opening of said clearance and forms an opening on said internal base formation schedule field, Introduce the impurity of the 2nd conductivity type into said collector field front face of said opening circles which consist of said 1st and 2nd sidewall layers, and an external base region is formed in said collector layer front face. The internal base region which is made to activate the impurity ion of the 2nd conductivity type injected into said collector field front face, and is connected with said external base region is formed. The manufacture approach of the semiconductor device characterized by having the process which said internal base region front face is made to diffuse the impurity of the 1st conductivity type, and forms an emitter region in it, and forming said opening on said internal base region.
[Claim 11] The process which forms the collector field which consists of a semi-conductor of the 1st conductivity type, and the process which forms the base electrode which consists of a polish recon layer by which the impurity of the 2nd conductivity type was doped on said collector field, The process which etches alternatively said predetermined insulating layer and said 1st predetermined base electrode of a location on said collector field, and forms opening after forming the 1st insulating layer in the whole surface, The process which forms the 2nd insulating layer in said collector field top in said opening, and said base-electrode side attachment wall, The process which injects the impurity ion of the 2nd conductivity type into said collector field front face of said opening circles alternatively by using said 1st insulating layer as a mask, The process which forms a sidewall layer in the side attachment wall of said 1st and 2nd insulating layers of said opening circles, By the process which injects the impurity ion of the 1st conductivity type into said collector field front face of said opening circles alternatively by using said the 1st insulating layer and said sidewall layer as a mask, and heat treatment Diffuse the impurity of the 2nd conductivity type from said base electrode, and an external base region is formed in said collector layer front face. The process which forms the internal base region which is made to

activate the impurity ion of the 2nd conductivity type injected into said collector field front face, and the 1st conductivity type, and is connected with said external base region, and the emitter region of said internal base region front face, respectively, The difference of an etch rate with said 1st insulating layer and said sidewall layer is used. The process which carries out etching removal of said 2nd insulating layer alternatively, and forms a gap between said internal base region front face and said sidewall layer base, After forming a conductive layer in the whole surface, closing opening of said clearance and forming an opening on said internal base region, patterning is carried out to a predetermined configuration. The manufacture approach of the semiconductor device characterized by having the process which forms an emitter electrode on said emitter region in said opening, and forming said opening on said internal base region.

[Translation done.]

TECHNICAL FIELD

[Industrial Application]
This invention relates to a semiconductor device and its manufacture approach.
It follows on detailed-ization of the component by improvement in the degree of integration of a semiconductor integrated circuit in recent years, and concentration of the local electric field in a component is becoming remarkable. Consequently, the hot carrier occurred in the field which a heavy current community concentrates, and the problem of reducing the dependability of a component has occurred. Then, it has been a big technical problem how the dependability fall of the component by the hot carrier is prevented.

[Translation done.]

PRIOR ART

[Description of the Prior Art]
Generating of the hot electron in the conventional semiconductor device is explained.
In the conventional MOS transistor, in order to prevent relaxation of electric-field concentration, and degradation of the component property by the hot electron, as shown in Fig. 16 (a), LDD (Lightly Doped Drain-souce) structure is used.
That is, n mold source and the drain field 25 which consist of dual structure of n-mold low concentration impurity range 23 and n+ mold high concentration impurity range 24 are formed in p-type silicon substrate 21 front face of the active element field detached by the component of field oxide 22, and LDD structure is made by it. On the channel field 26 inserted into n-mold low concentration impurity range 23 of these n mold source and the drain field 25, the gate electrode 28 is formed through gate oxide 27. Moreover, the sidewall layer 29 is formed in this gate electrode 28 side attachment wall. Furthermore, the insulating layer 31 has accumulated on the whole surface, and the source and the drain electrode 32 are formed through the contact aperture which carried out opening to this insulating layer 31 on n+ mold high concentration impurity range 24 of n mold source and the drain field 25.
Thus, since n mold source and the drain field 25 have dual structure of n-mold low concentration impurity range 23 and n+ mold high concentration impurity range 24, concentration of a heavy current community [/ especially near the drain field] was eased, and generating of a hot electron has been controlled.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]
Since the insulating layer itself by which the hot carrier generated to the field which a heavy current community concentrates by preparing an opening or preparing an opening through an insulating thin film on the field which a heavy current community concentrates locally [a semi-conductor substrate] is poured in, and a trap is carried out does not exist as mentioned above according to this invention, it is lost that a hot carrier is cumulatively accumulated into the insulating layer on the field which a heavy current community concentrates.
Also in the field which a heavy current community which a hot carrier generates concentrates by this, the fall of the property of the component by generating of a hot carrier and dependability can be prevented.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]
However, with detailed-izing of a semiconductor device, relaxation of electric-field concentration becomes less enough also in the MOS transistor of the above-mentioned conventional LDD structure, and the improvement is needed.
That is, in the MOS transistor of the conventional LDD structure, the channel 64 which is a path as a current is formed in channel field 26 front face of the gate electric field impressed to the gate electrode 28 at the time of the actuation, and a current comes to flow between n mold source and the drain field 25.
However, in order that big electric field may concentrate near the drain field especially, in this part, a carrier, for example, an electron, is accelerated greatly. And if the kinetic energy comes to have the kinetic energy exceeding 1/2KT (K shows a Boltzmann's constant and T shows absolute temperature.), it will become the so-called hot electron. Since the probability of the collision in the channel field of a carrier becomes small, an electron is accelerated so much by channel length's shortening accompanying detailed-izing of a component, and the probability of occurrence of a hot electron becomes large by it. In this way, according to modification of the course by the collision with the semi-conductor atom near the drain, and an operation of the Coulomb force from the gate electrode 28, the generated hot electron comes to be poured into the sidewall layer 29 interior of gate electrode 28 side attachment wall of LDD structure, as shown in Fig. 16 (b).
Thus, if the amount of charges by which was injected into sidewall layer 29 base and the trap was carried out increases gradually, p form reversal of the n-mold low concentration impurity range 23 front face will be carried out, and it will come to check the flow of channel current. The property and dependability of a MOS transistor will fall according to such a mechanism.
Moreover, also in a bipolar mold transistor, degradation of a component occurs according to the case of a MOS transistor, and a similar mechanism in near the interface an emitter touches the base.
For example, it explains using the bipolar mold transistor of the self aryne (Self-align) structure which makes base resistance small and makes parasitic capacitance, such as capacity between the collector-bases, small.
the sectional view showing [17] this bipolar mold transistor (a), and Fig. 17 (b) -- the -- it is an enlarged drawing a part.
n+ mold collector pad layer 42 is embedded on the p-type silicon substrate 41, n-mold collector field 43 and n+ mold collector contact field 45 are separated and formed of field oxide 44 on this n+ mold collector pad layer 42, p+ mold external base region 46 and the interior base region 47 of p-mold are formed in n-mold collector field 43 front face, and n+ mold emitter region 48 is formed in interior base region of p-mold 47 front face. And on p+ mold external base region 46 and n+ mold emitter region 48, the base cash-drawer electrode 49 and the emitter cash-drawer electrode 50 which consist of a polish recon layer by which the impurity of p mold and n mold was doped, respectively are formed.
Moreover, on n+ mold collector contact field 45, the base cash-drawer electrode 49, and the emitter cash-drawer electrode 50, the collector electrode 52, the base electrode 53, and the emitter electrode 54

which consist of aluminum, respectively are formed through the contact aperture which carried out opening of the whole surface to the wrap insulating layer 51.
A depletion layer will be formed in a part for the joint of the interior base region 47 of p-mold, and n+ mold emitter region 48 if a reverse bias is now impressed between a base electrode 53 and the emitter electrode 54. Since the die length of the interior base region 47 of p-mold inserted into p+ mold external base region 46 and n+ mold emitter region 48 from the description of self aryne structure is short at this time, the width of face of the depletion layer formed is comparatively narrow. Therefore, if high electric field are impressed between base-emitters, it will be accelerated by this high electric field, and the carrier opposite-generated within the depletion layer will turn into a hot carrier. And the part is poured in into the insulating layer 51 on the interior base region 47 of p-mold, and a trap is carried out. For example, if the trap of the electron hole is carried out into an insulating layer 51, interior base region of p-mold 47 front face will carry out n form reversal, base resistance will become high, as a result the recombination in a surface space-charge region will increase, and a current amplification factor hFE will be reduced.
Thus, also in a bipolar mold transistor, degradation of the component property by generating of a hot carrier arises like a MOS transistor.
Then, this invention aims at offering the semiconductor device which can prevent the fall of the property of the component by the hot carrier, and dependability, and its manufacture approach also in the field which a heavy current community which a hot carrier generates concentrates.

[Translation done.]

MEANS

[The means for solving a technical problem]
Figs. 1 and 2 are principle explanatory views of this invention, respectively.
In Fig. 1 , the field 12 which a local heavy current community concentrates on semi-conductor substrate 11 front face is formed. Concentration of such a heavy current community is generated in the depletion layer formed in the pn junction to which the strong reverse bias was impressed, for example etc. And although the insulating layer 13 is formed on the semi-conductor substrate 11, the opening 14 is formed between field 12 front faces and insulating-layer 13 bases which the heavy current community of this semi-conductor substrate 11 concentrates.
Thus, this invention has the description in the point that the opening 14 is formed on the field 12 which the heavy current community of the semi-conductor substrate 11 concentrates.
Next, actuation is explained.
Now, the carrier opposite-generated in the field 12 which the carrier poured in into the field 12 which a heavy current community concentrates, or a heavy current community concentrates turns into a hot carrier which is accelerated by this heavy current community and has big kinetic energy. And this hot carrier collides with the semi-conductor atom in the field 12 which a heavy current community concentrates, and changes a course. If an operation of Coulomb force is added at this time, for example, the semi-conductor substrate 11 upper part, the probability of course modification to the upper part to the fixed direction will become high especially.
However, since the opening 14 is formed on the field 12 which this heavy current community concentrates, a hot carrier runs out of the field 12 which a heavy current community concentrates, and it runs through an opening 14, and is not poured into an insulating layer 13. That is, on the field 12 which a heavy current community concentrates, since the insulating layer 13 which carries out the trap of the hot carrier does not exist, even if a hot carrier occurs, are recording of a charge does not arise, therefore neither a property nor dependability is reduced.
Moreover, in Fig. 2 , an insulating layer 13 is formed on the semi-conductor substrate 11, and that the opening 14 is formed between field 12 front faces and insulating-layer 13 bases which the heavy current community of the semi-conductor substrate 11 concentrates, although it is the same as Fig. 1 , the insulating thin film 15 is formed on the above-mentioned field 12 which the heavy current community in this **** 14 concentrates.
Thus, the opening 14 may be formed through the insulating thin film 15 on the field 12 where a heavy current community concentrates this invention.
Next, actuation is explained.
Since the insulating thin film 15 is formed on the field 12 which a heavy current community concentrates, some hot carriers generated by the heavy current community are accumulated into the insulating thin film 15. However, since the upper part serves as [the thickness] an opening 14 very thin, the insulating thin film 15 will not produce are recording of the charge beyond it, if the amount of charges accumulated in the insulating thin film 15 can be controlled very small and the charge of a constant rate is accumulated.

Therefore, it becomes possible by controlling this amount of stored charge below to a predetermined value to reduce a property and dependability.
Moreover, when it is not desirable to expose field 12 front face which the heavy current community of the semi-conductor substrate 11 concentrates to a vacuum or air, the front face is protected by existence of the insulating thin film 15.

[Translation done.]

OPERATION

[Function]
Since the insulating layer itself by which the hot carrier generated to the field 12 which a heavy current community concentrates by forming an opening 14 or forming an opening 14 through the insulating thin film 15 on the field 12 which a heavy current community concentrates locally is poured in, and a trap is carried out does not exist, this invention of a hot carrier being cumulatively accumulated into an insulating layer is lost.
Degradation of the property of the semiconductor device resulting from the hot carrier which this generates in the field which a heavy current community concentrates, and dependability can be prevented.

[Translation done.]

EXAMPLE

[Example]
Hereafter, based on the example illustrating this invention, it explains concretely.
(1) the 1st example the sectional view showing the MOS transistor according [Fig. 3 (a)] to the 1st example of this invention, and Fig. 3 (b) -- the -- it is an enlarged drawing a part.
P-type silicon substrate 21 front face is detached by field oxide 22 by the component. And n mold source and the drain field 25 which consist of dual structure of n-mold low concentration impurity range 23 and n+ mold high concentration impurity range 24 are formed in p-type silicon substrate 21 front face of the active element field, and LDD structure is made. On the channel field 26 inserted into n-mold low concentration impurity range 23 of these n mold source and the drain field 25, the gate electrode 28 is formed through gate oxide 27.
Moreover, the sidewall layer 29 is formed in this gate electrode 28 side attachment wall. And the description of this example is in the point that the opening 30 is formed in this sidewall layer 29 lower part. Therefore, n-mold low concentration impurity range 23 top of n mold source and the drain field 25 serves as an opening 30, and the sidewall layer 29 does not exist.
Furthermore, the insulating layer 31 has accumulated on the whole surface, and opening of this opening 30 is closed. And the source and the drain electrode 32 are formed through the contact aperture which carried out opening to this insulating layer 31 on n+ mold high concentration impurity range 24 of n mold source and the drain field 25.
Thus, since the opening 30 is formed between n-mold low concentration impurity range 23 front face of n mold source and the drain field 25, and sidewall layer 29 base according to the 1st example, Even if the hot electron generated by heavy current community concentration collides with a semi-conductor atom and changes a course Even if it receives an operation of the Coulomb force from the gate electrode 28, it jumps out of n-mold low concentration impurity range 23 front face, it runs through an opening 14, and a trap is not poured in and carried out to the sidewall layer 29.
Moreover, since the charge by which the trap was carried out can exist only in the distance ****** sidewall layer 29 of an opening 30 even if it escapes from an opening 30 and the trap of some hot electrons is carried out to the sidewall layer 29, a trap charge can exert an operation of Coulomb force on a substrate only from the place from which only the part of an opening 14 was separated. therefore, the effect is boiled markedly and becomes small.
Therefore, even if the probability of occurrence of a hot electron becomes large by channel length's shortening accompanying detailed-izing of a component, it can prevent that n-mold low concentration impurity range 23 front face carries out p form reversal, and the property and dependability of a MOS transistor of LDD structure fall with the amount of charges by which was injected into sidewall layer 29 base and the trap was carried out.
Next, the manufacture approach by the 1st example of a MOS transistor shown in Fig. 3 is explained using Fig. 4 .
Wet oxidation of the whole surface is carried out to the active element field of the p-type silicon substrate 21 at the temperature of 900 degrees C by using as a mask the pad oxide film with a thickness

of 200A and the CVD nitride with a thickness of 1000A which carried out the laminating, and field oxide 22 with a thickness of about 5000A is formed in it. Then, after phosphoric acid voile and HF (fluoric acid) remove a CVD nitride and a pad oxide film, respectively, gate oxide 27 with a thickness of 50-300A is formed by HCl (hydrochloric acid) oxidation on the p-type silicon substrate 21 of the active element field separated by field oxide 22 (refer to Fig. 4 (a)).
Subsequently, after depositing with a thickness of 4000A polish recon layer 28a on the whole surface (refer to Fig. 4 (b)), patterning of this polish recon layer 28a that diffuses p mold or n mold impurity, and gives conductivity is carried out to a predetermined configuration, and the gate electrode 28 is formed (refer to Fig. 4 (c)). Then, As(arsenic)+ ion is poured in on condition that acceleration voltage 60keV and dose 3x1013cm-2 by using field oxide 22 and the gate electrode 28 as a mask. This forms n-mold low concentration impurity range 23 in p-type silicon substrate 21 front face (refer to Fig. 4 (d)).
Subsequently, after growing up a CVD nitride with a thickness of 500-1000A and a CVD oxide film with a thickness of 2000-3000A in order, the sidewall layer 34 which perform anisotropic etching, and the CVD nitride 33 is made to remain on gate electrode 28 side attachment wall and this about 28 gate electrode gate oxide 27, and consists of a CVD oxide film on this CVD nitride 33 is formed.
Then, As+ ion is poured in on condition that acceleration voltage 60keV and dose 1-5x1015cm-2 by using field oxide 22, the gate electrode 28, the CVD nitride 33, and the sidewall layer 34 as a mask, and n+ mold high concentration impurity range 24 is formed in p-type silicon substrate 21 front face.

DESCRIPTION OF DRAWINGS

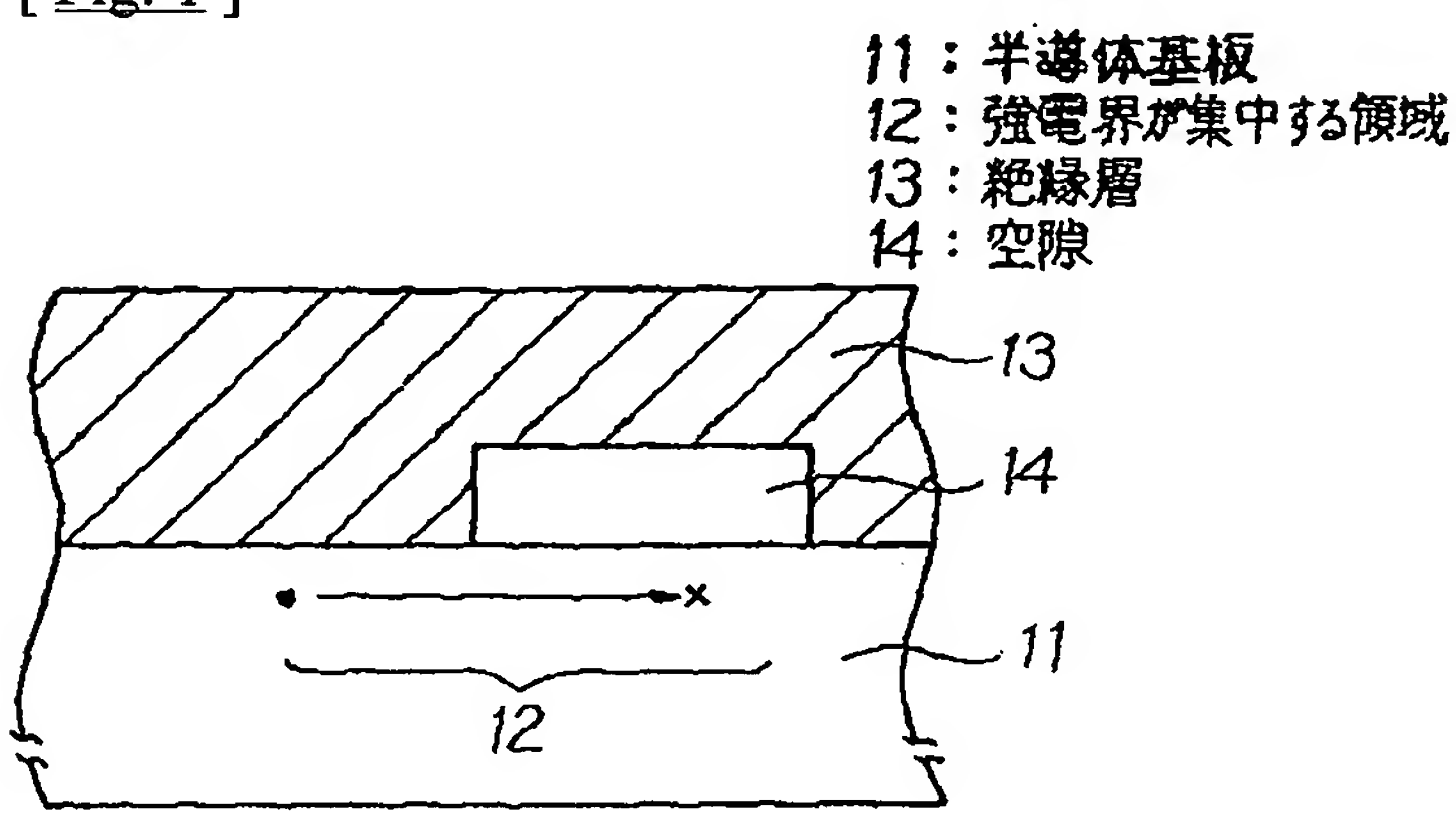
[Brief Description of the Drawings]
Figs. 1 and 2 are principle explanatory views of this invention,
Fig. 3 is a sectional view showing the MOS transistor by the 1st example of this invention,
Fig. 4 is process drawing for explaining the manufacture approach by the 1st example of a MOS transistor shown in Fig. 3 ,
Fig. 5 is process drawing for explaining the manufacture approach by the 2nd example of a MOS transistor shown in Fig. 3 ,
Fig. 6 is process drawing for explaining the manufacture approach by the 3rd example of a MOS transistor shown in Fig. 3 ,
Fig. 7 is a sectional view showing the MOS transistor by the 2nd example of this invention,
Fig. 8 is process drawing for explaining the manufacture approach by the 1st example of a MOS transistor shown in Fig. 7 ,
Fig. 9 is process drawing for explaining the manufacture approach by the 2nd example of a MOS transistor shown in Fig. 7 ,
Fig. 10 is process drawing for explaining the manufacture approach by the 3rd example of a MOS transistor shown in Fig. 7 ,
Fig. 11 is process drawing for explaining the manufacture approach by the 4th example of a MOS transistor shown in Fig. 7 ,
Fig. 12 is a sectional view showing the bipolar mold transistor by the 3rd example of this invention,
Fig. 13 is process drawing for explaining the manufacture approach of the bipolar mold transistor shown in Fig. 12,
Fig. 14 is a sectional view showing the bipolar mold transistor by the 4th example of this invention,
Fig. 15 is process drawing for explaining the manufacture approach of the bipolar mold transistor shown in Fig. 14,
Fig. 16 is a sectional view showing the conventional MOS transistor,
Fig. 17 is a sectional view showing the conventional bipolar mold transistor.
In drawing,
11 .... Semi-conductor substrate,
12 .... Field which a heavy current community concentrates,
13, 31, 51, 51a .... Insulating layer,
14, 30, 55 .... Opening,
15, 39, 40 .... Insulating thin film,
21 41 .... P-type silicon substrate,
22 44 .... Field oxide
23 .... n-mold low concentration impurity range,
24 .... n+ mold high concentration impurity range,
25 .... n mold source, drain field,
26 .... Channel field,

27 .... Gate oxide
28 .... Gate electrode,
28a .... Polish recon layer,
29, 34, 35, 37, 38, 60, 61 .... Sidewall layer,
30a, 55a .... Clearance,
32 .... The source, drain electrode,
33 56 .... CVD nitride,
36 58 .... Silicon oxide
42 .... n+ mold collector pad layer,
43 .... n-mold collector field,
45 .... n+ mold collector contact field,
46 .... p+ mold external base region,
47 .... Interior base region of p-mold,
48 .... n+ mold emitter region,
49 .... Base cash-drawer electrode,
50 .... Emitter cash-drawer electrode,
52 .... Collector electrode
53 .... Base electrode
54 62 .... Emitter electrode,
57 .... Opening,
59 .... B+ ion,
63 .... aluminum layer,
64 .... Channel.

[Translation done.]

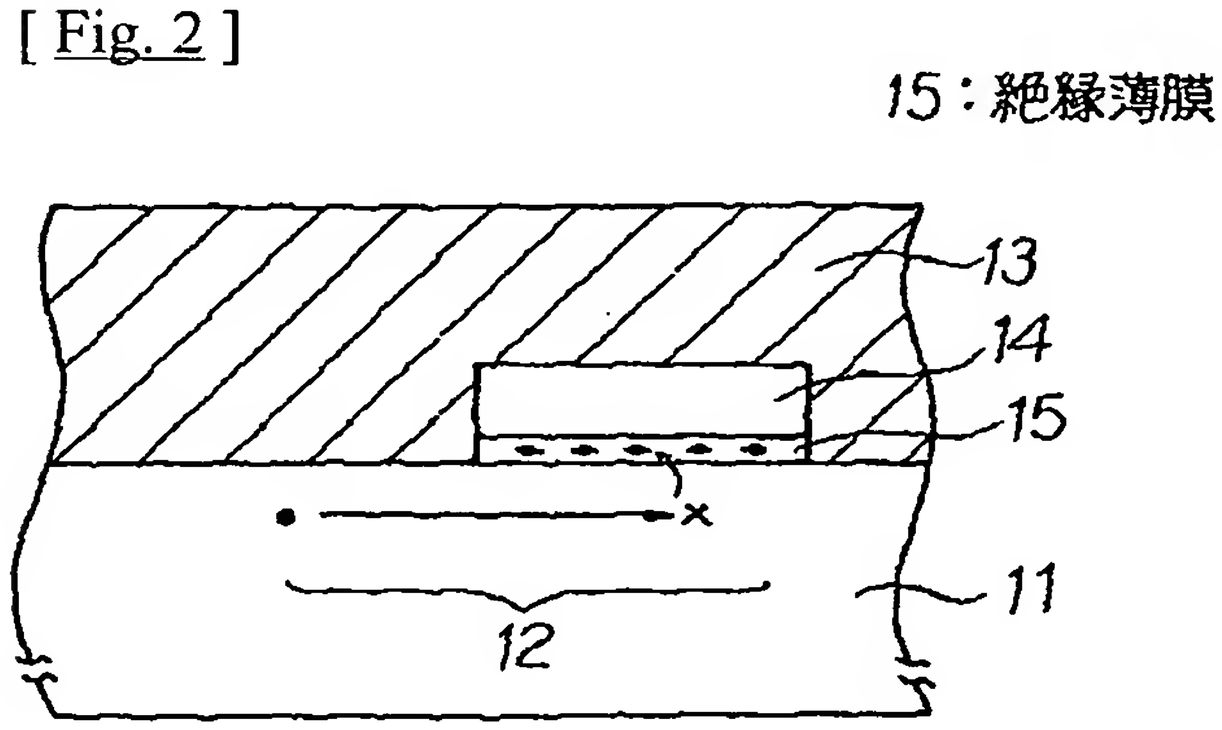
DRAWINGS

[Fig. 1]



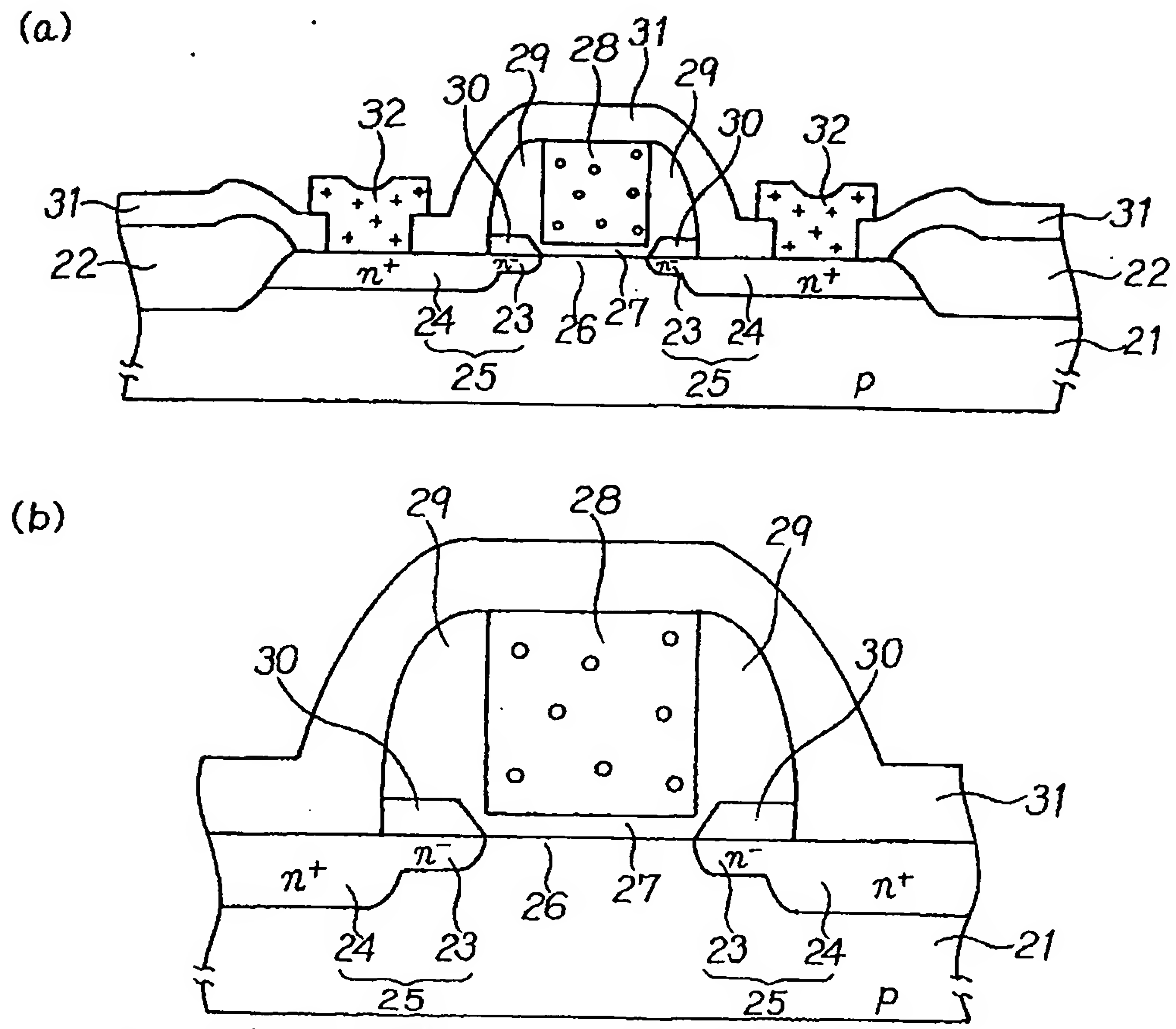
本発明の原理説明図

[Fig. 2]



本発明の原理説明図

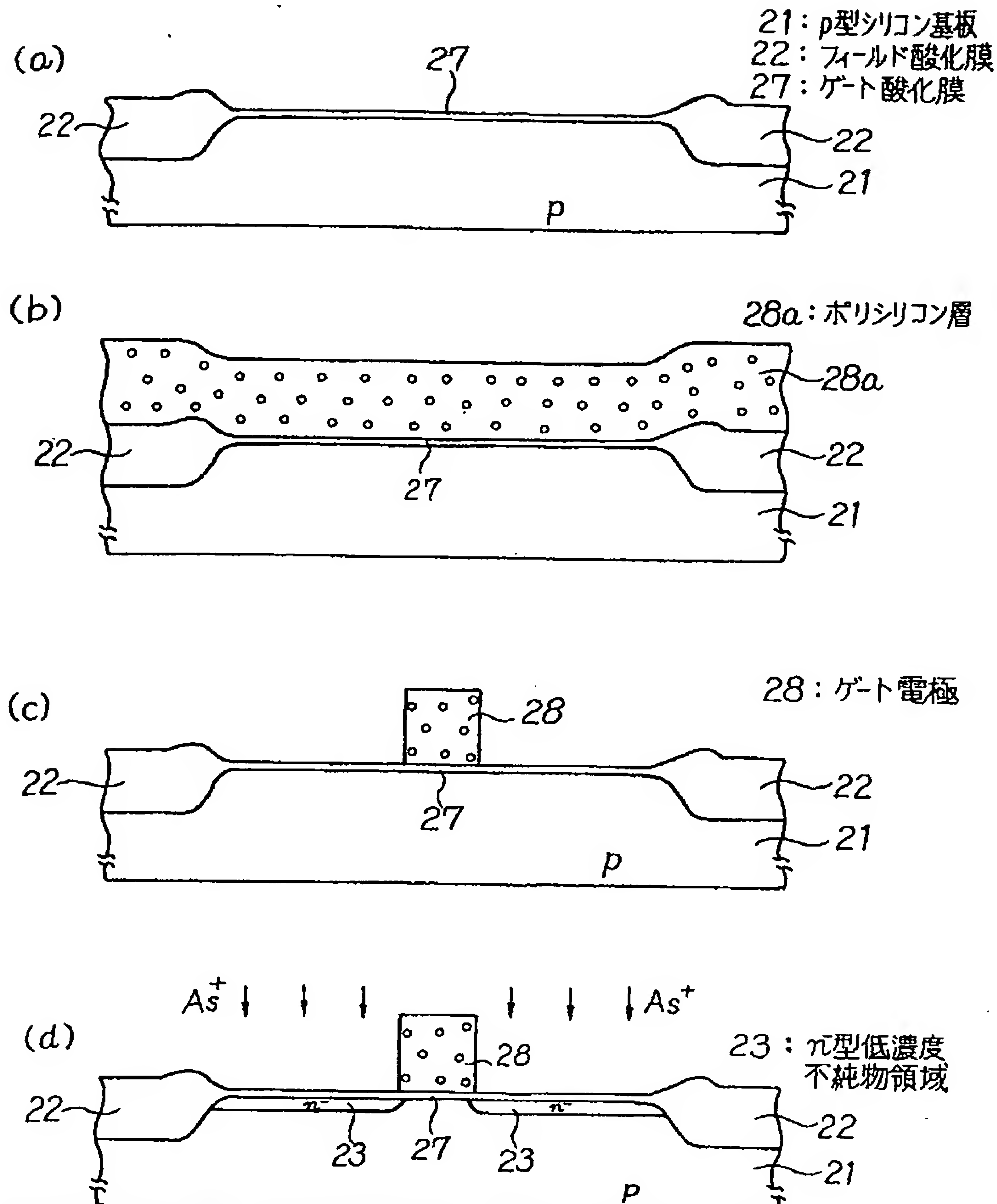
[Fig. 3]



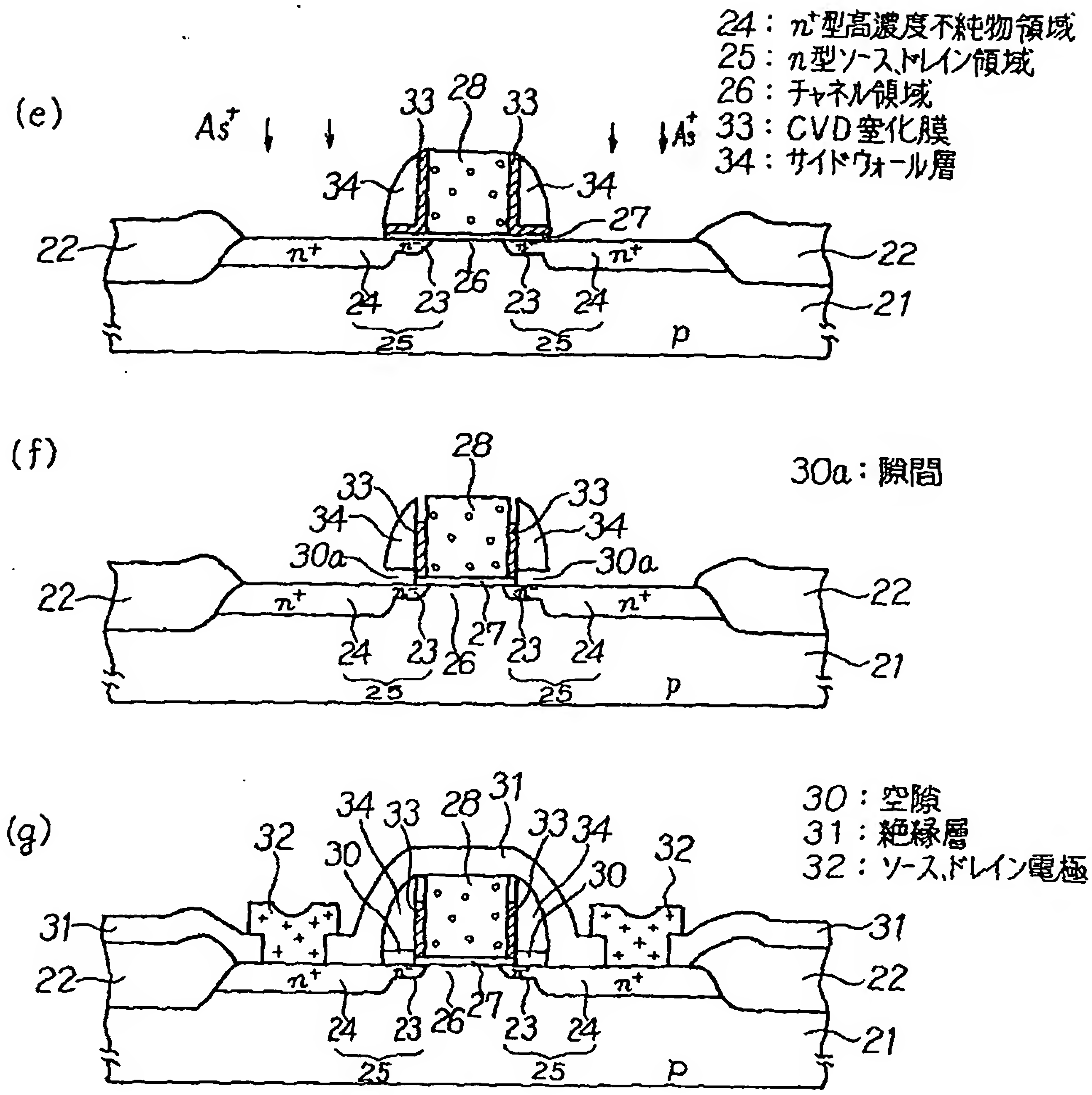
21：p型シリコン基板
22：フィールド酸化膜
23：n^-型低濃度不純物領域
24：n^+型高濃度不純物領域
25：n型ソース、ドレイン領域
26：チャネル領域
27：ゲート酸化膜
28：ゲート電極
29：サイドウォール層
30：空隙
31：絶縁層
32：ソース、ドレイン電極

本発明の第1の実施例によるMOS型トランジスタを示す断面図

[Fig. 4]

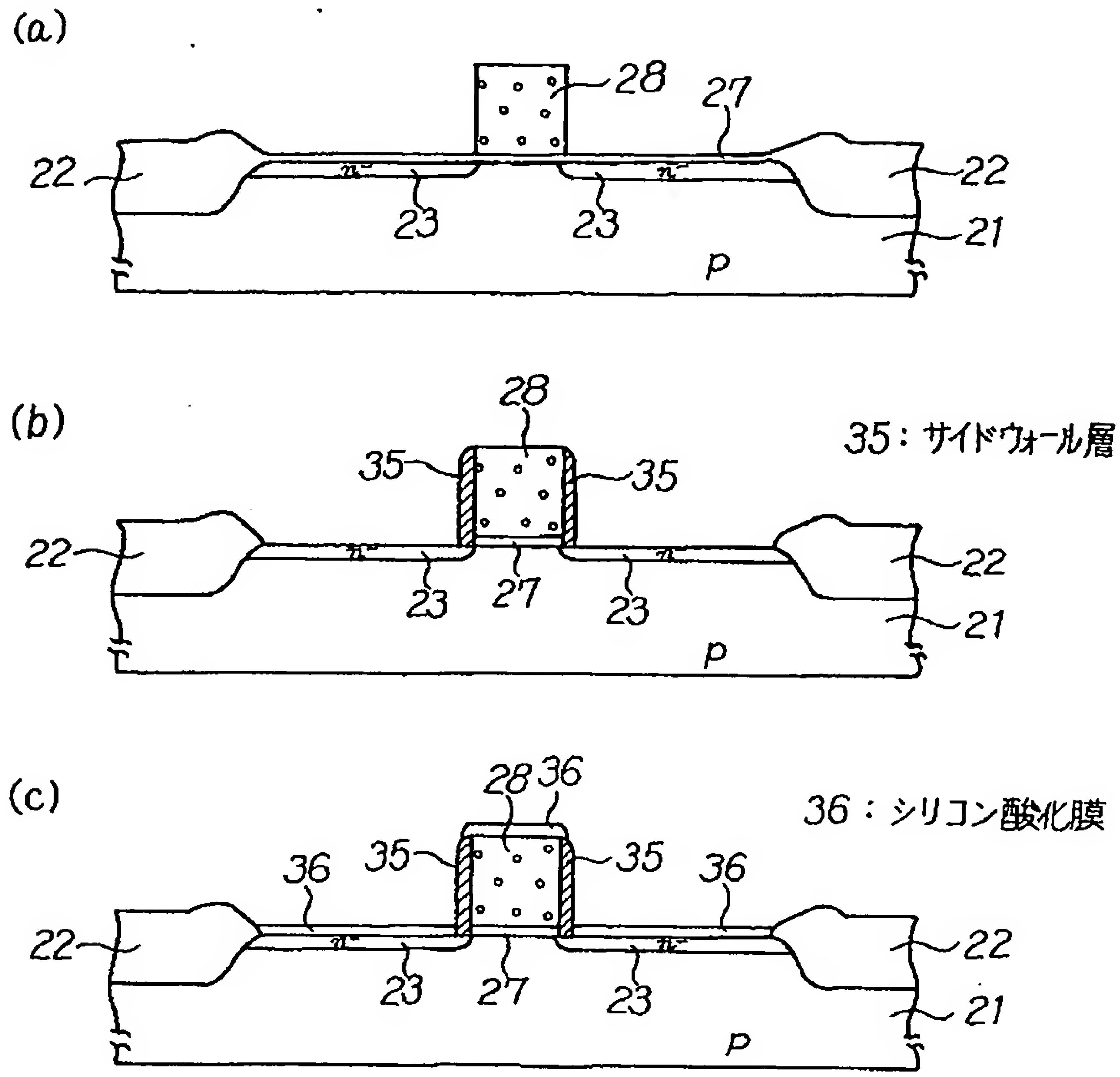


第3図に示すMOS型トランジスタの第1の例による製造方法を説明するための工程図

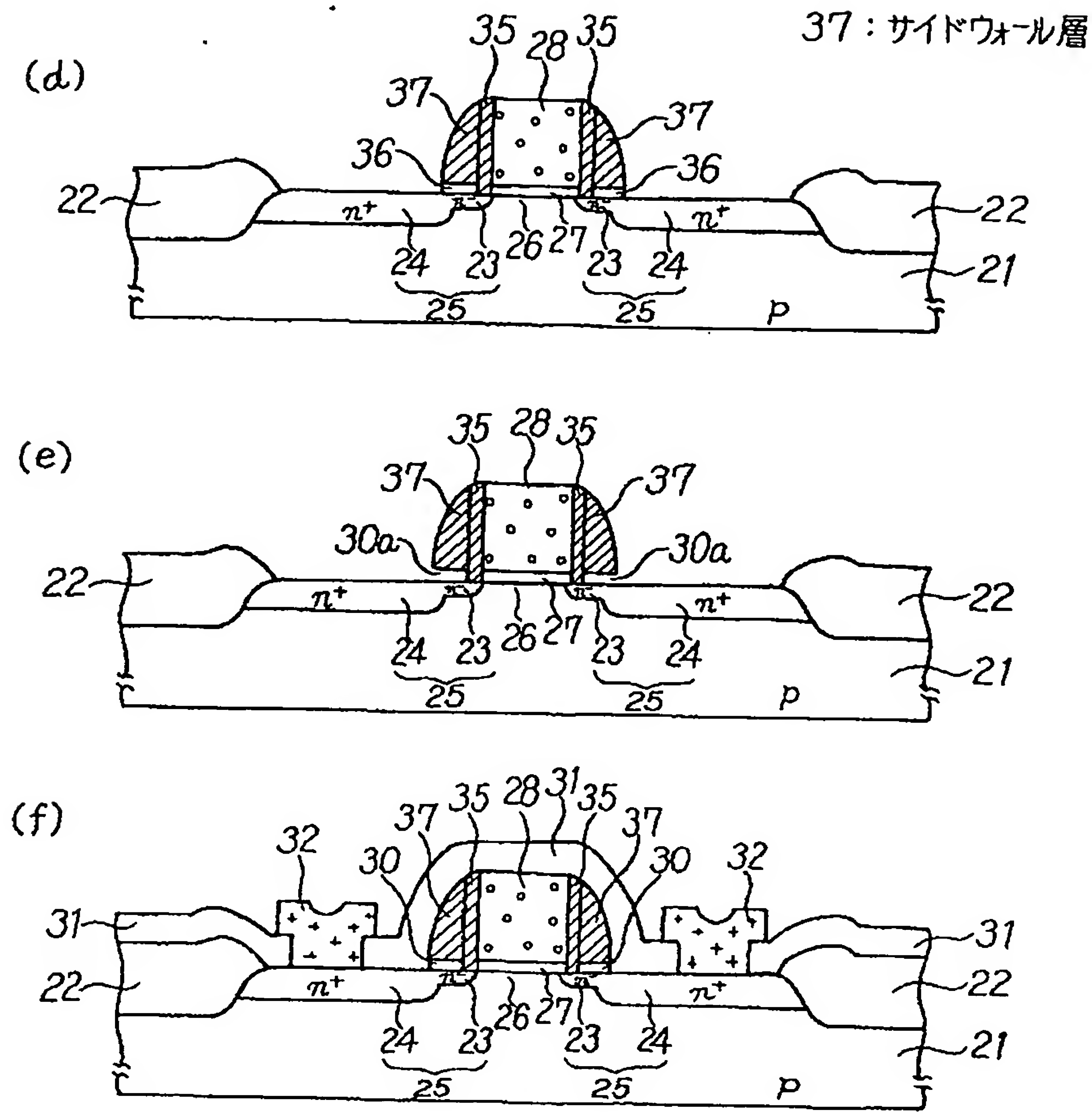


第3図に示すMOS型トランジスタの
第1の例による製造方法を説明するための工程図

[Fig. 5]

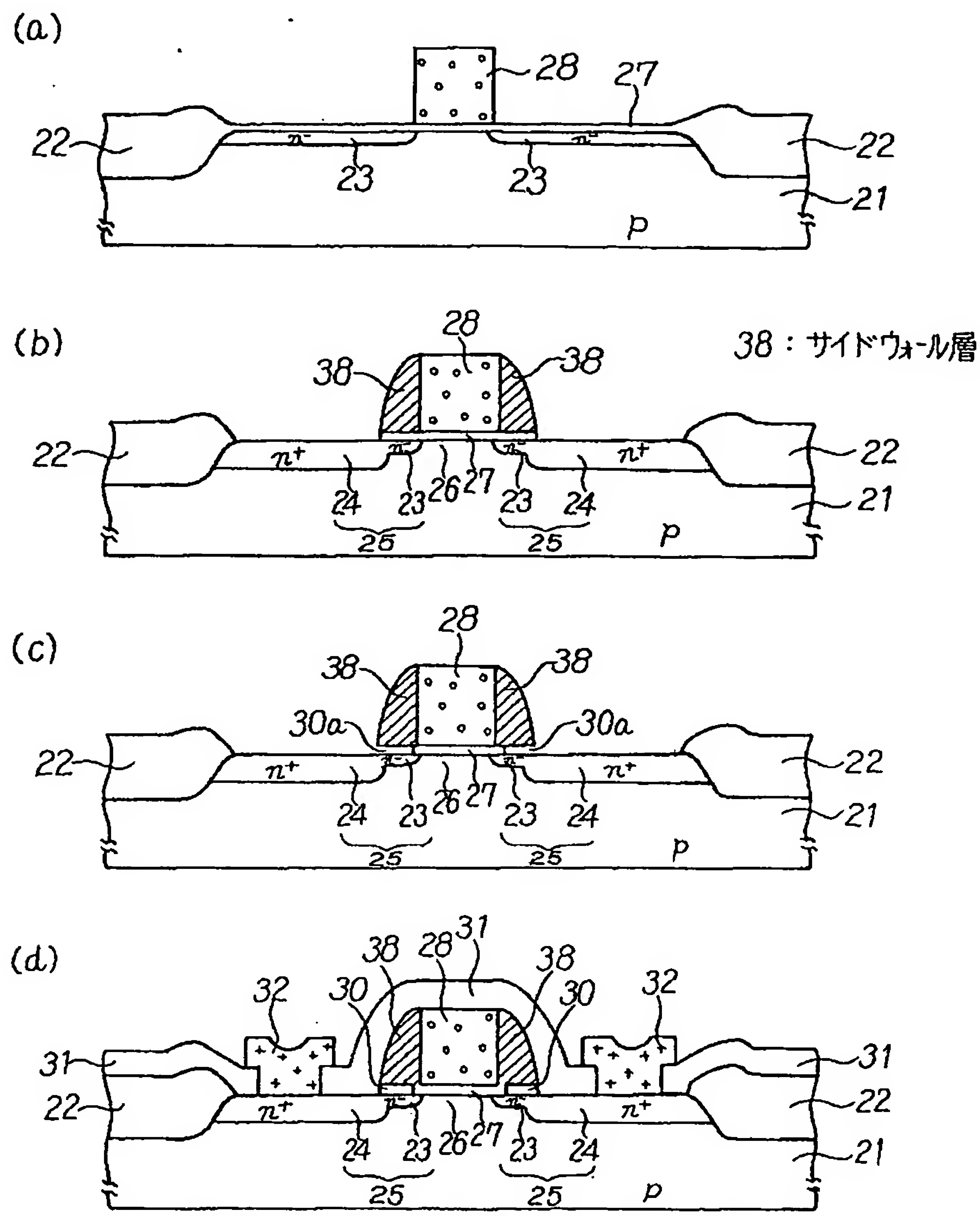


第3図に示すMOS型トランジスタの
第2の例による製造方法を説明するための工程図



第3図に示すMOS型トランジスタの
第2の例による製造方法を説明するための工程図

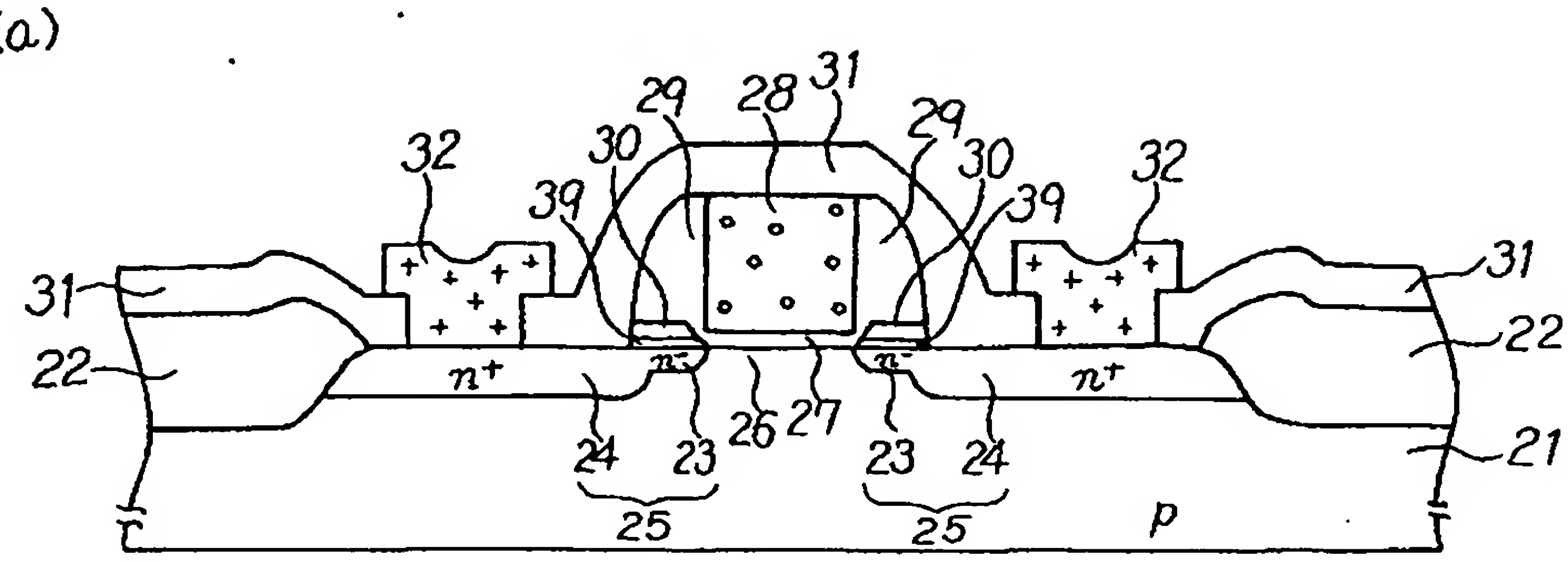
[Fig. 6]



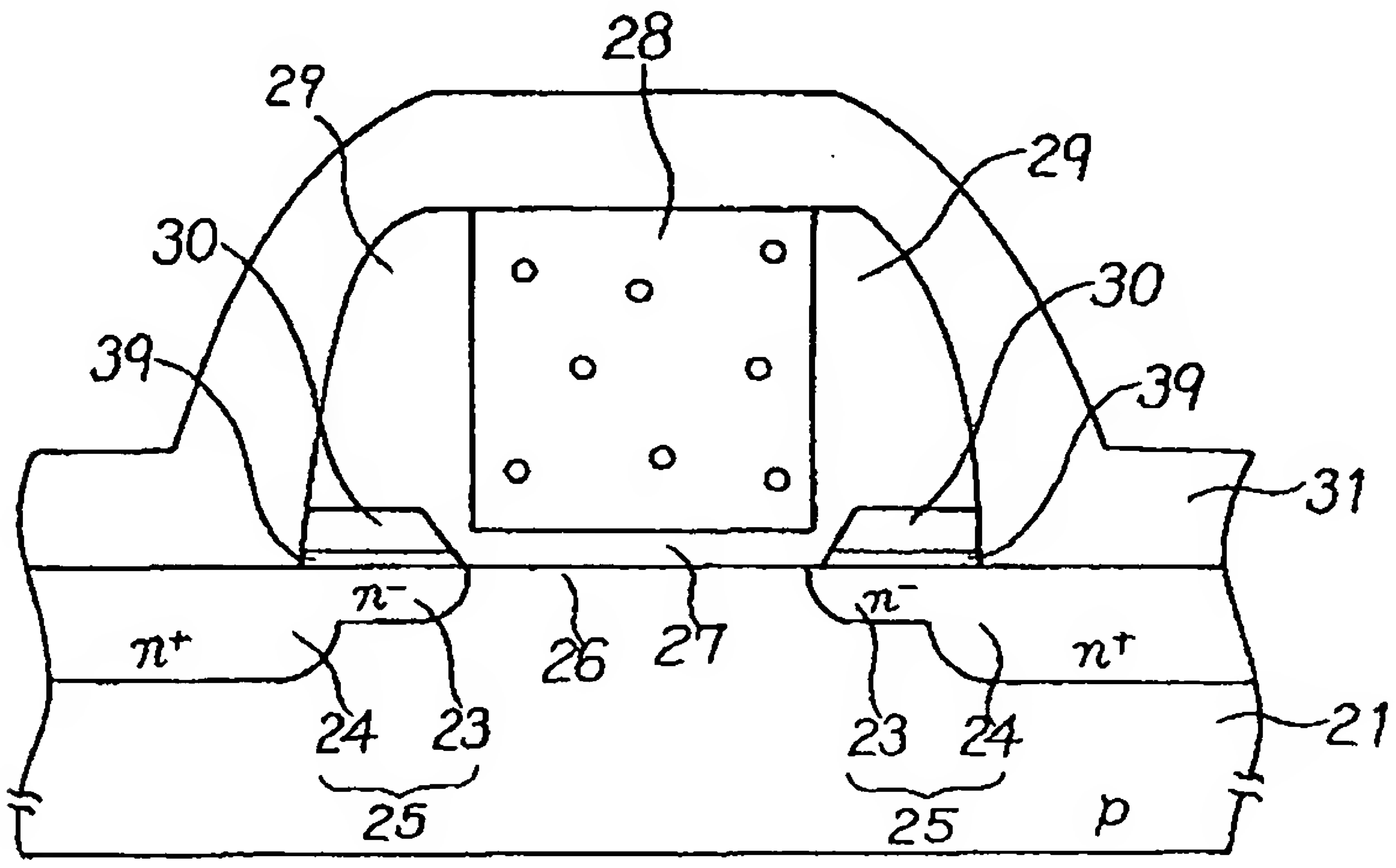
第3図に示すMOS型トランジスタの
第3の例による製造方法を説明するための工程図

[Fig. 7]

(a)



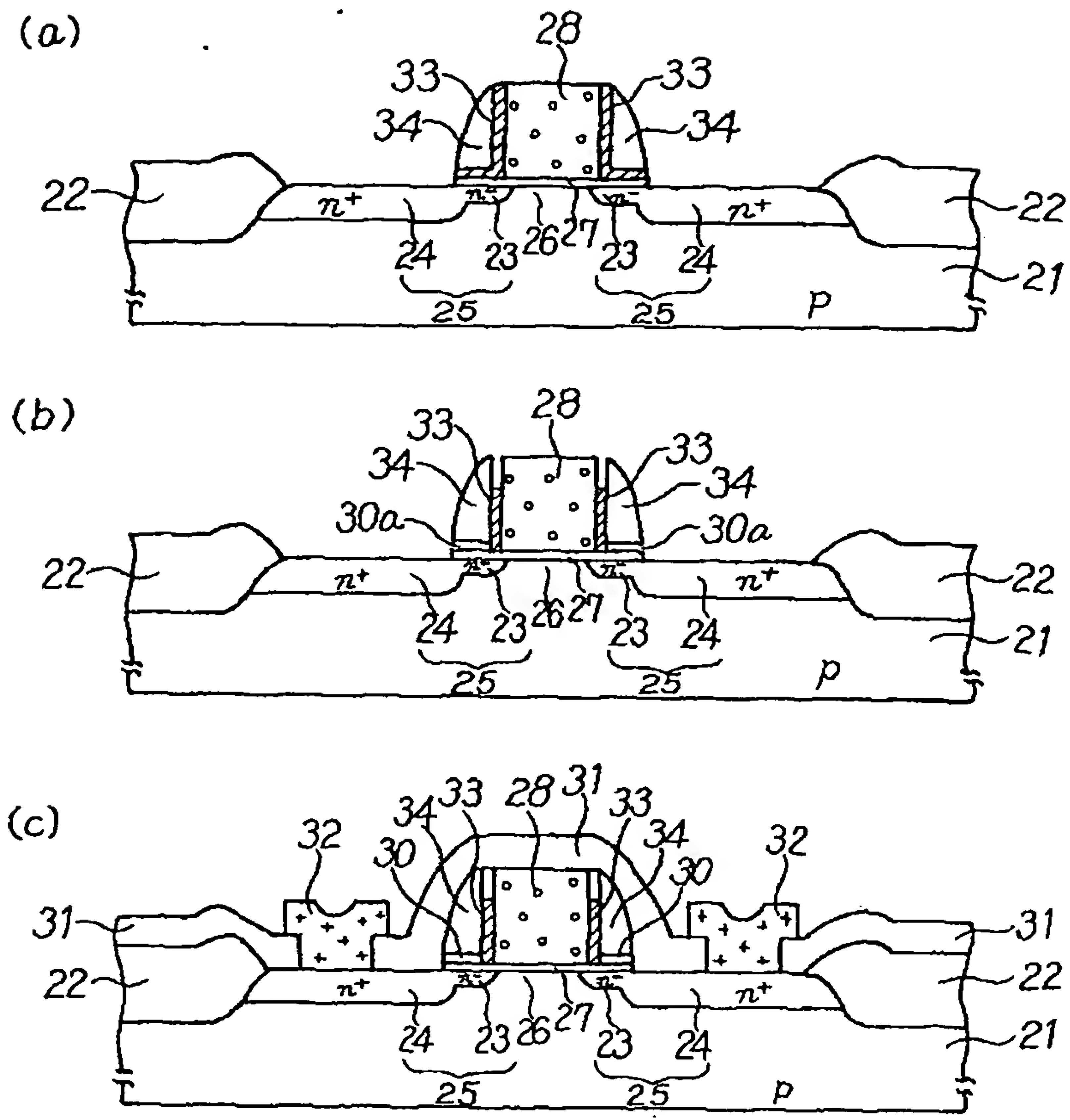
(b)



39：絶縁薄膜

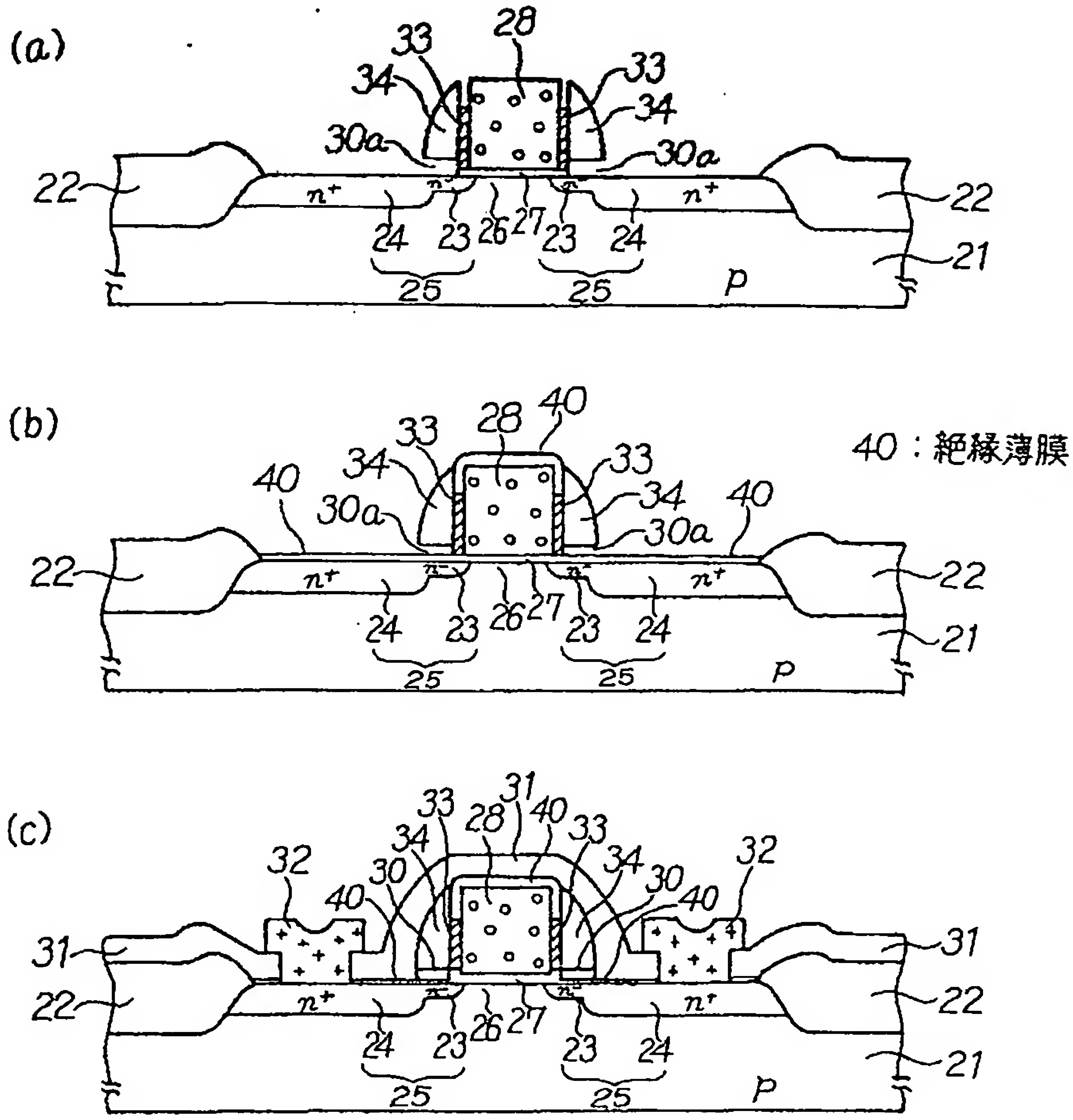
本発明の第2の実施例によるMOS型トランジスタを示す断面図

[Fig. 8]



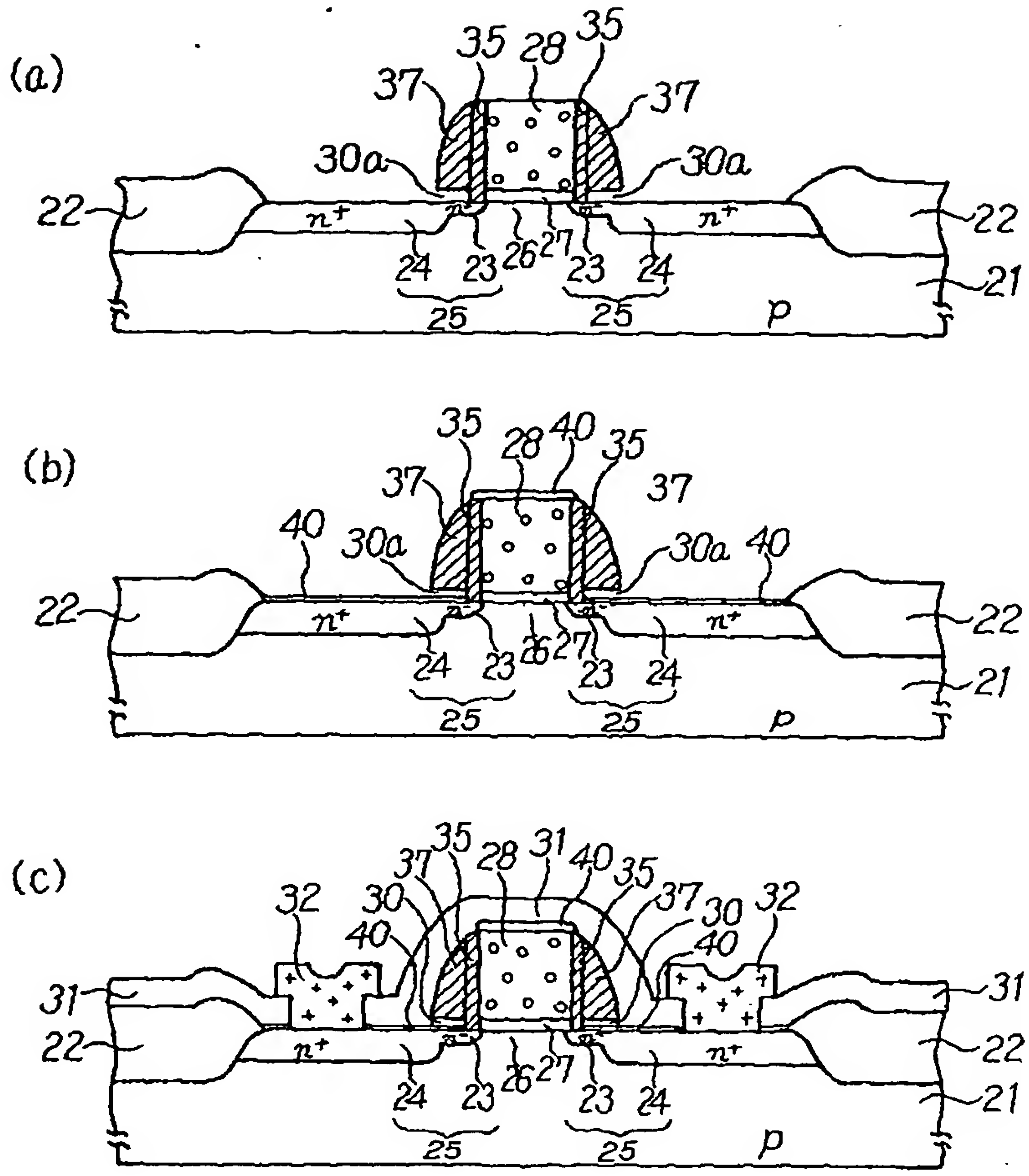
第7図に示すMOS型トランジスタの
第1の例による製造方法を説明するための工程図

[Fig. 9]



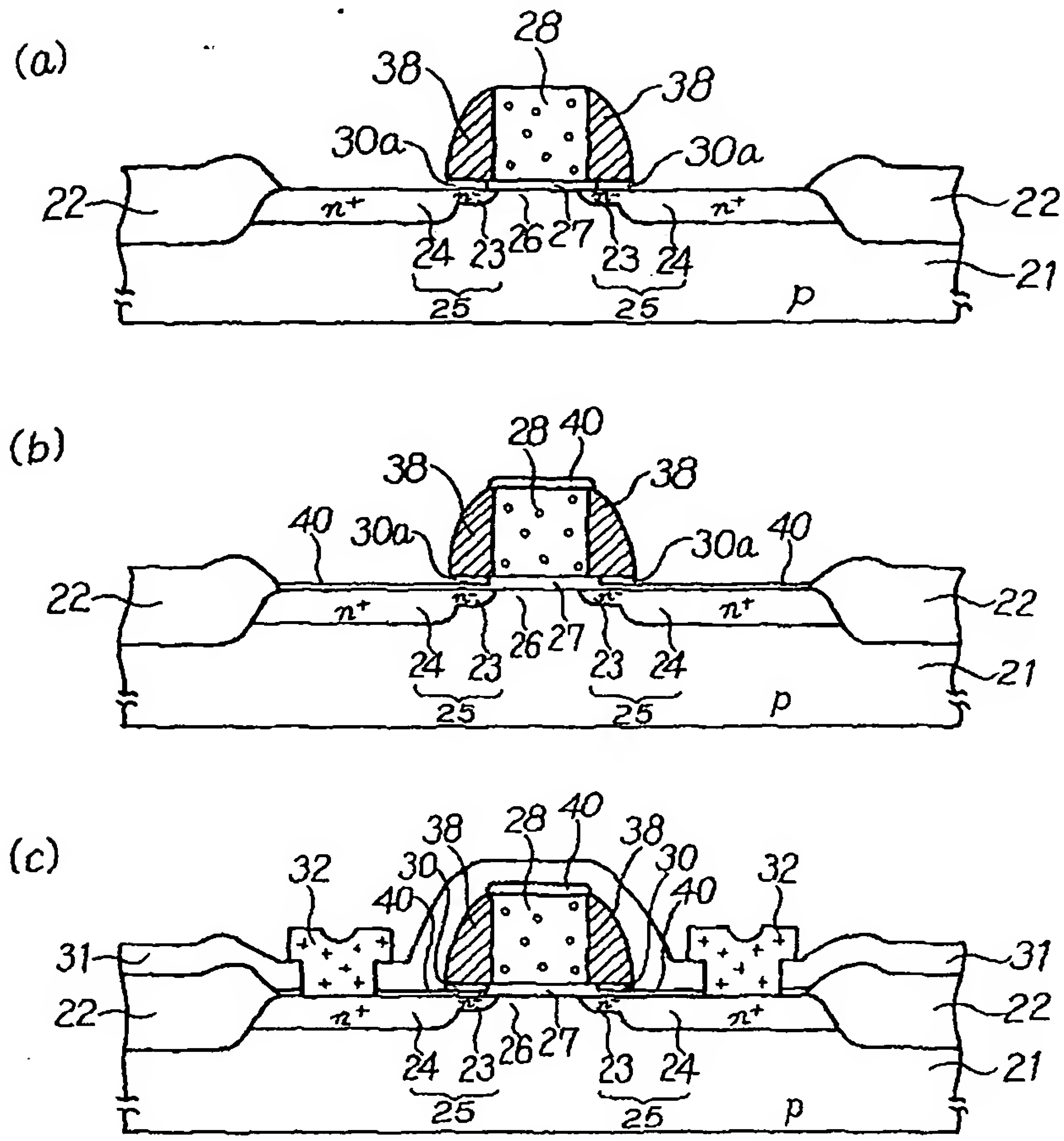
第７図に示すＭＯＳ型トランジスタの
第２の例による製造方法を説明するための工程図

[Fig. 10]



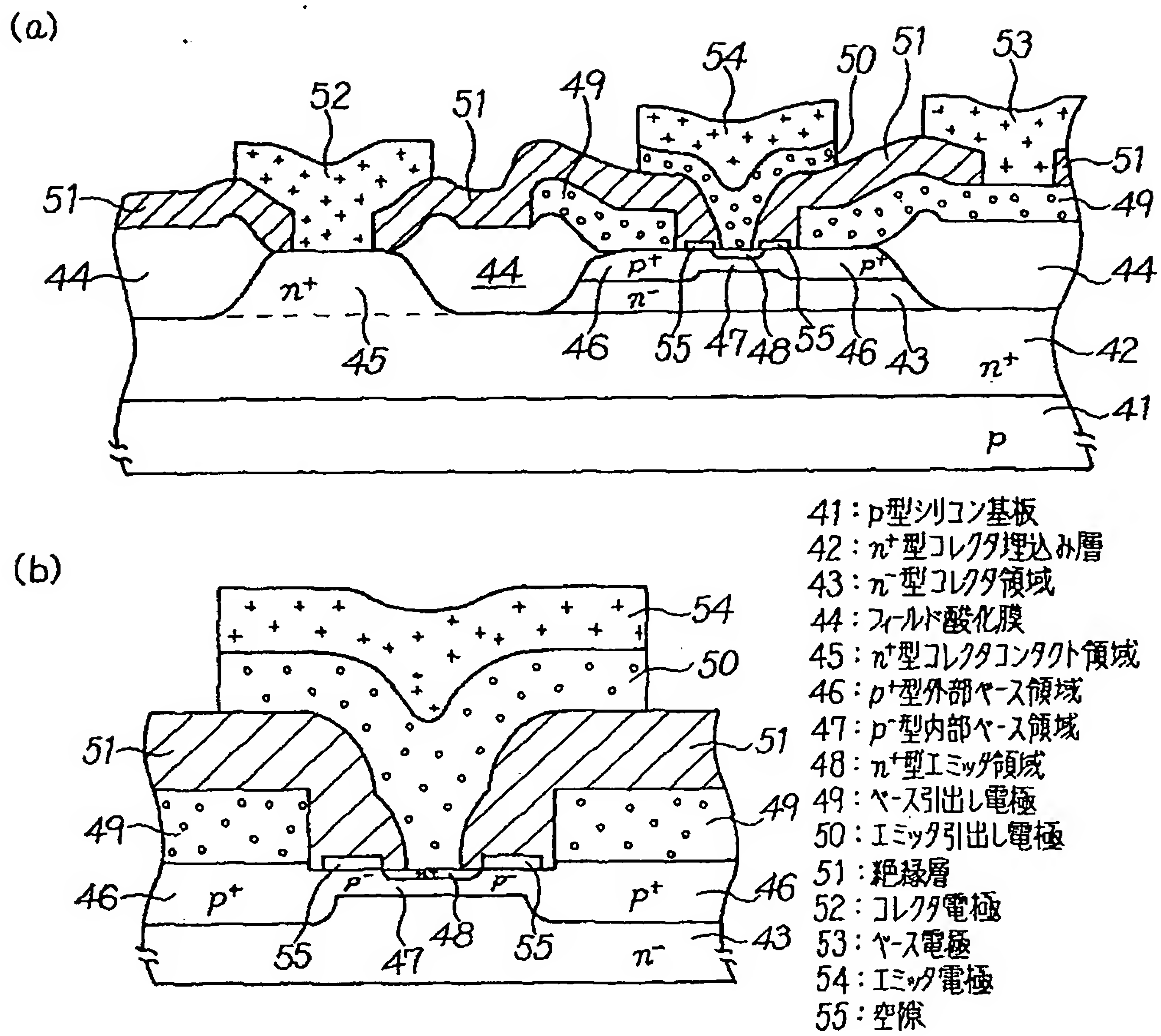
第７図に示すＭＯＳ型トランジスタの
第３の例による製造方法を説明するための工程図

[Fig. 11]



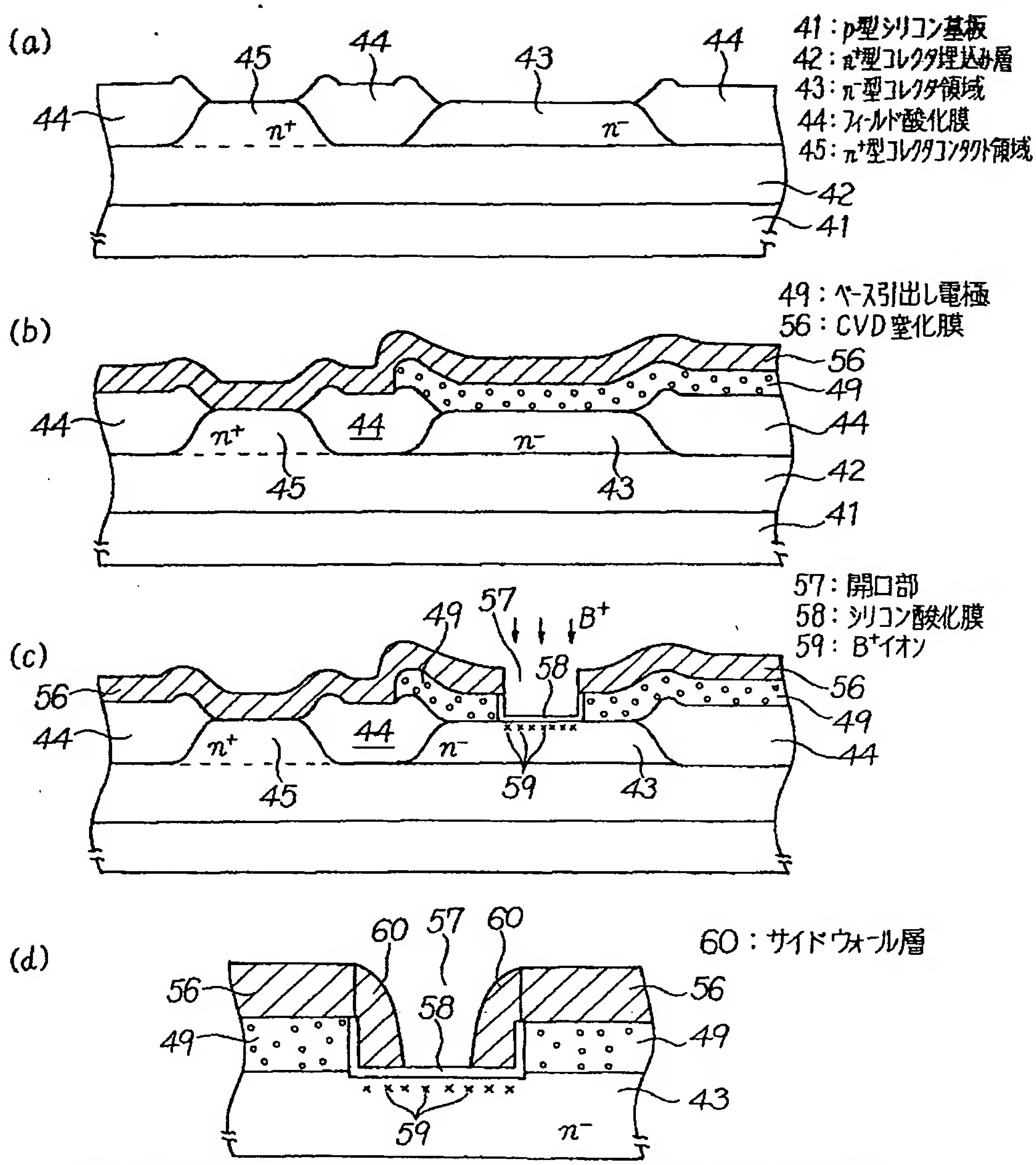
第7図に示すMOS型トランジスタの
第4の例による製造方法を説明するための工程図

[Fig. 12]

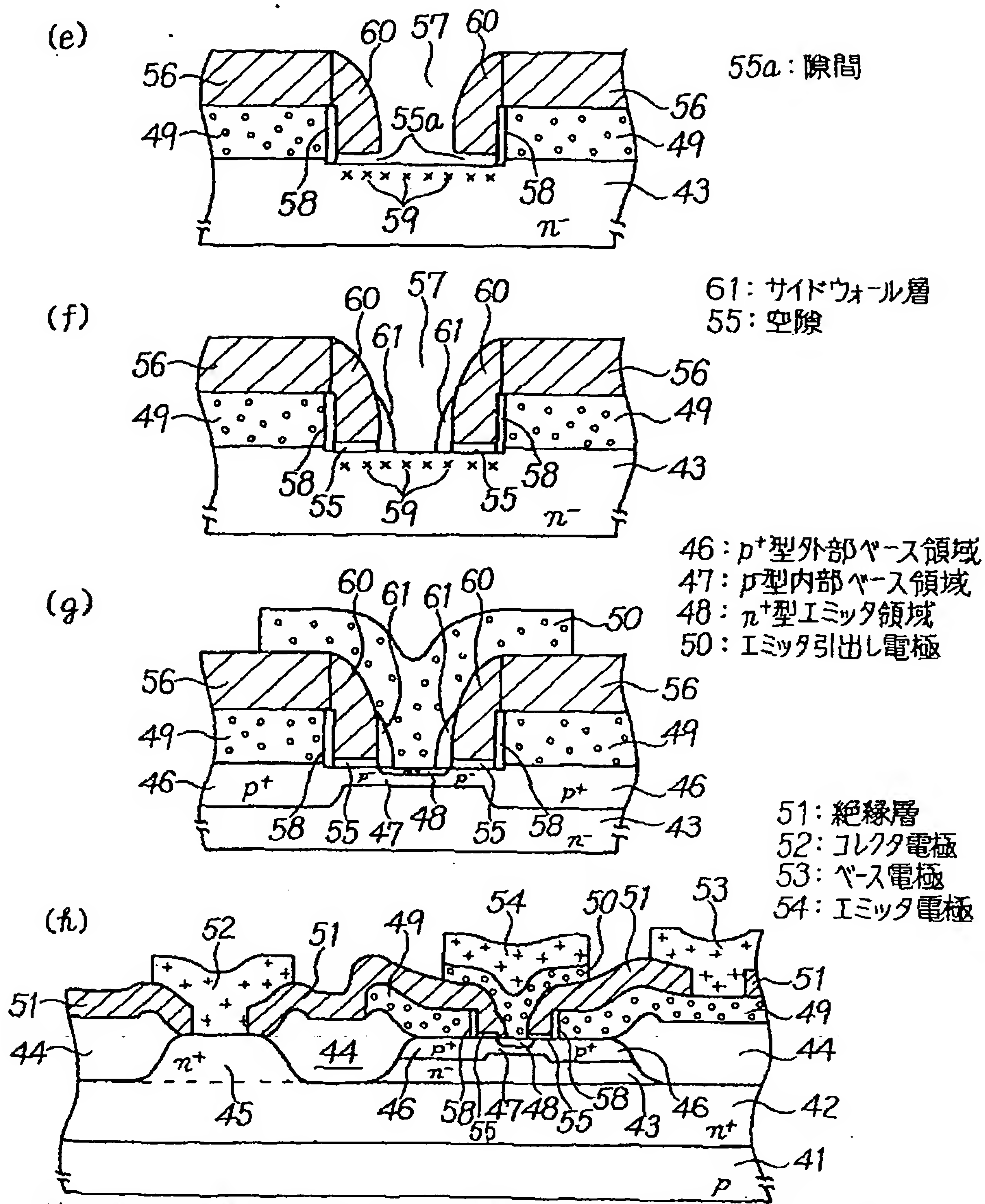


本発明の第3の実施例によるバイポーラ型トランジスタを示す断面図

[Fig. 13]



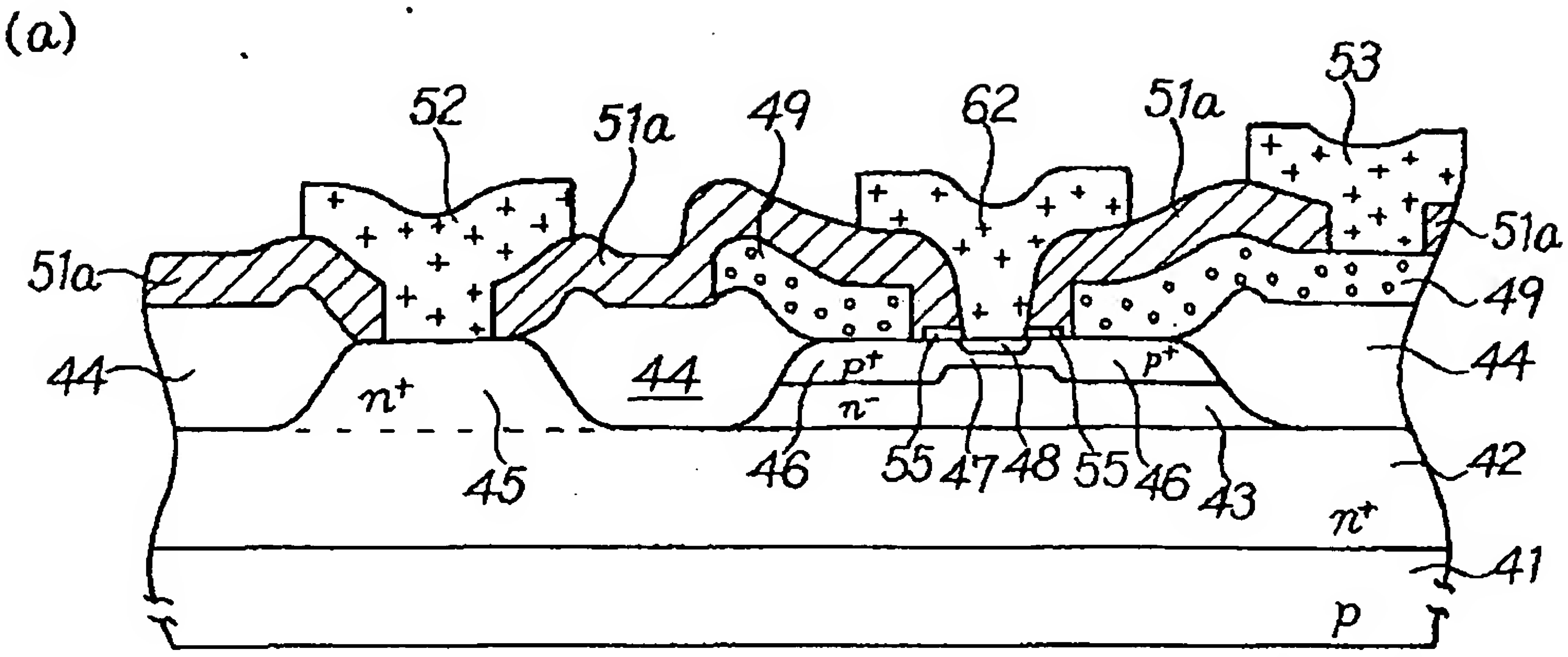
第12図に示すバイポーラ型トランジスタの製造方法を説明するための工程図



第12図に示すバイポーラ型トランジスタの製造方法を説明するための工程図

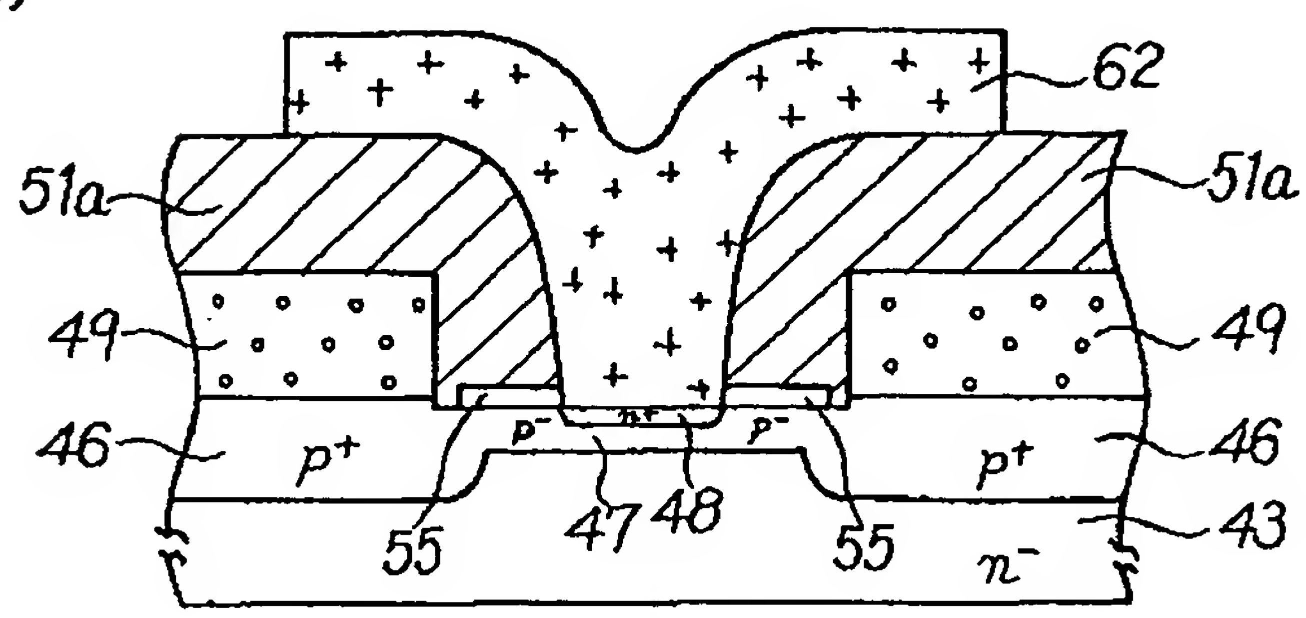
[Fig. 14]

(a)



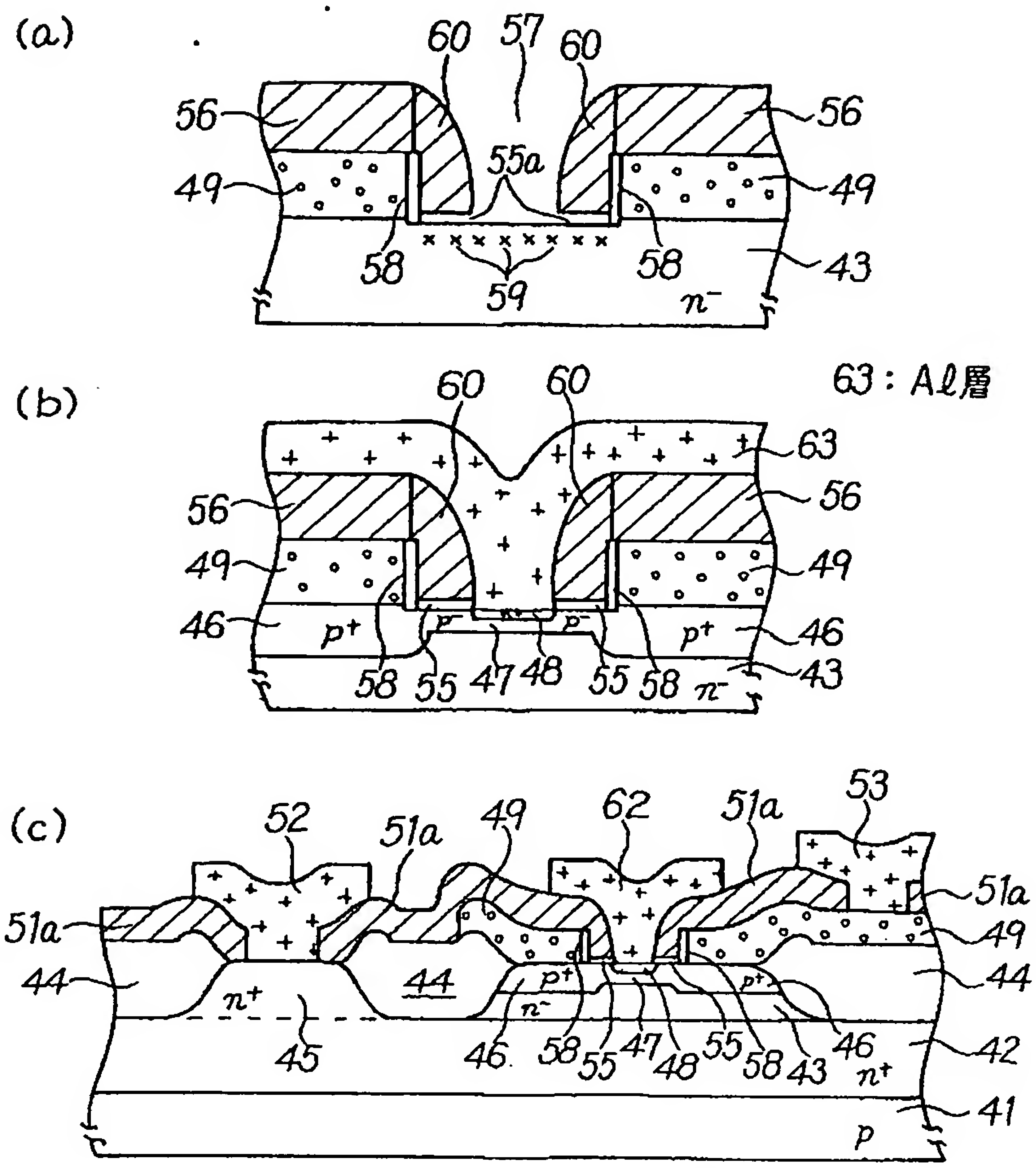
51a：絶縁層
62：エミッタ電極

(b)



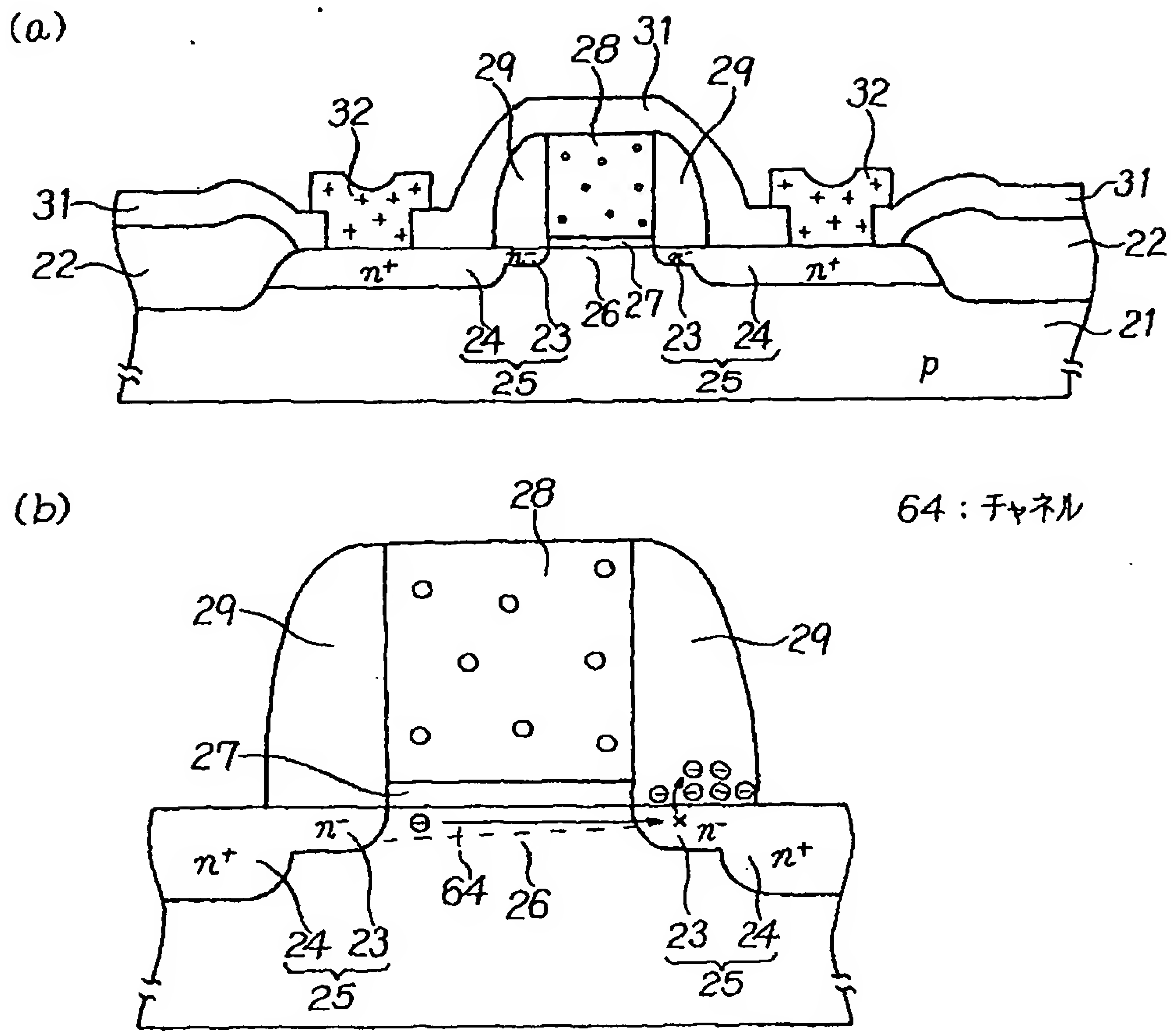
本発明の第４の実施例によるバイポーラ型トランジスタを示す断面図

[Fig. 15]



第14図に示すバイポーラ型トランジスタの製造方法を説明するための工程図

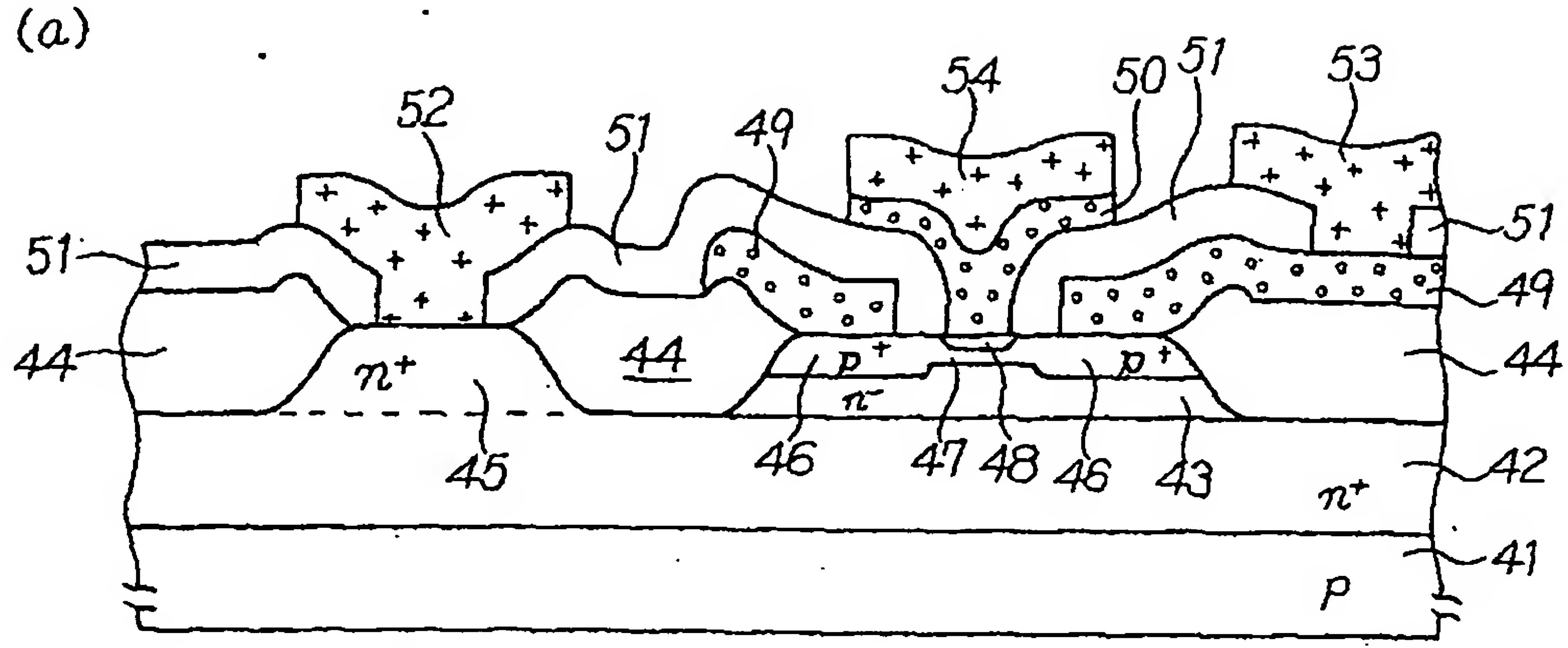
[Fig. 16]



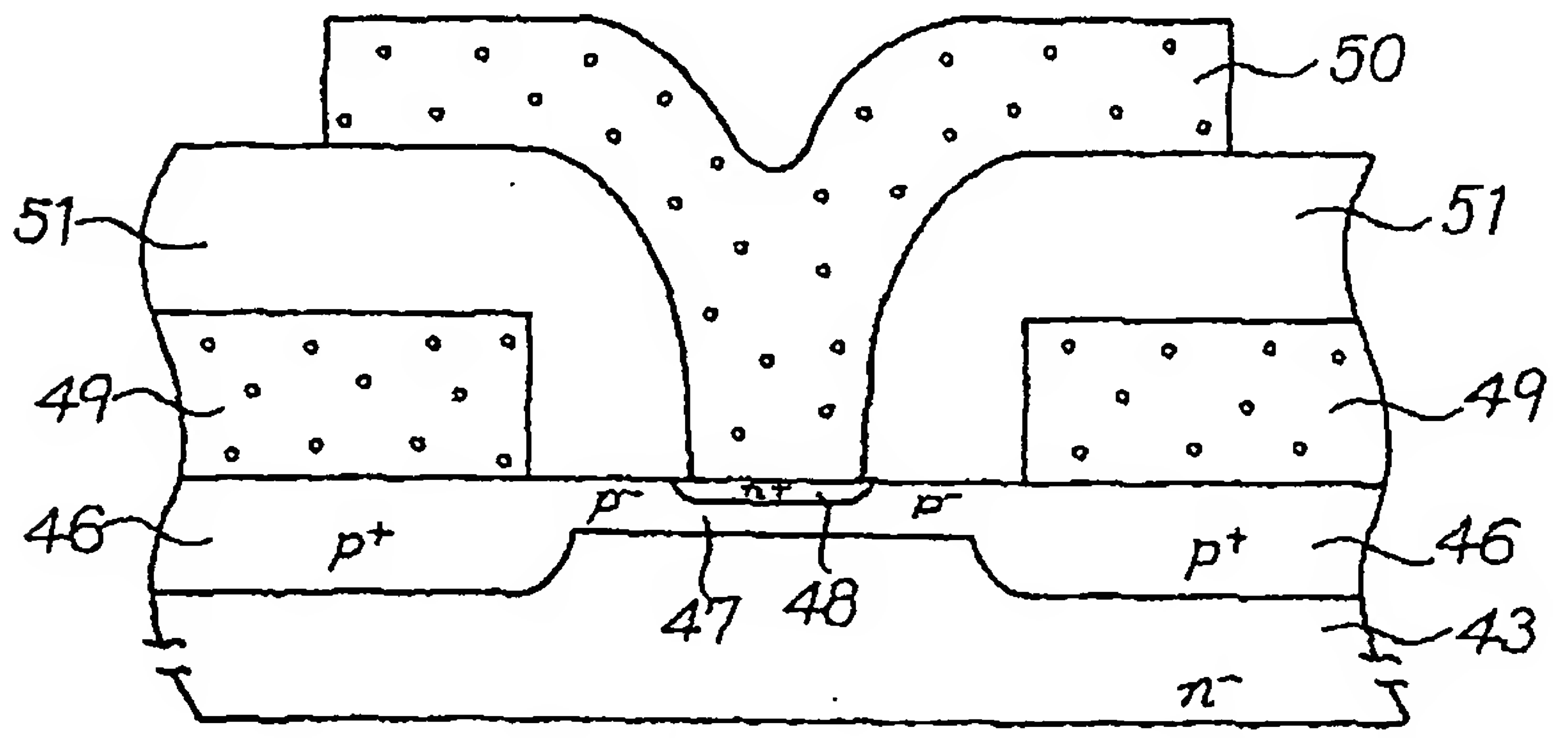
従来のＭＯＳ型トランジスタを示す断面図

[Fig. 17]

(a)



(b)



従来のバイポーラ型トランジスタを示す断面図

[Translation done.]